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HIGH STABILITY TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR STUDY--ETC(U)
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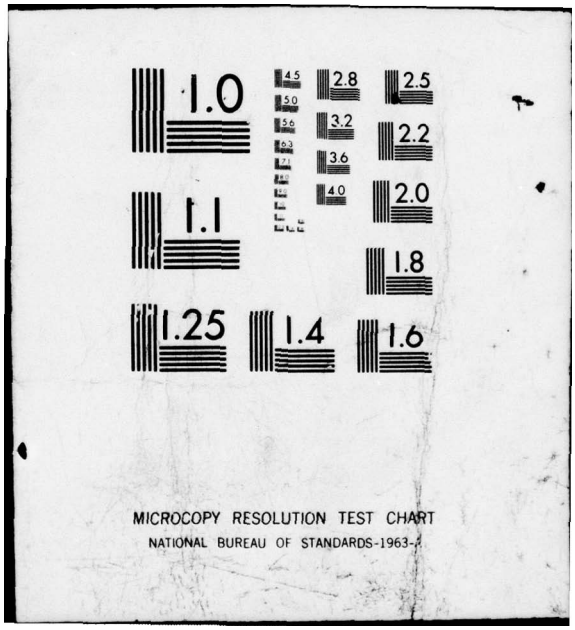
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Research and Development Technical Report

ECOM-73-0137-F

HIGH STABILITY TEMPERATURE COMPENSAT CRYSTAL OSCILLATOR STUDY

Alan Mroch and Glenn Hykes
Collins Radio Group
Rockwell International
Cedar Rapids, Iowa 52406

February 1977

Final Report for Period 28 February 1975 to 29 February 1976

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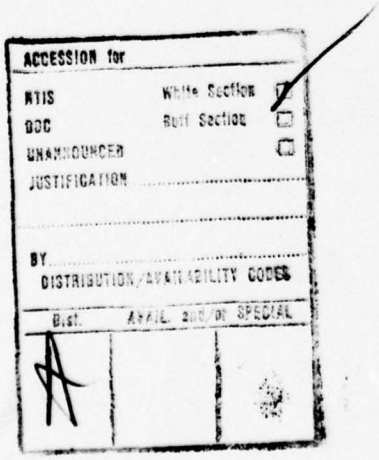

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A miniature high-stability tmperature-compensated crystal oscillator (HSTCXO) has been developed with new features for eventual use in SSB communications equipment. These new features are a wider temperature range for the same temperature stability (±5 pp 10^8 from -46 to +85°C), single supply (10 ±0.5 V), low power consumption (less than 100 mW), a CMOS compatible output (10 V square wave) and small size, 2.75 in X 1.5 in X 0.5 in (6.98 cm X 3.81 cm X 1.27 cm). Other important features of the HSTCXO are a 50-ohm output (0.125 V rms), insensitivity

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to load variations and voltage variations (±5 pp 10^9), and fast warmup (1 pp 10^8 of final frequency in 1 minute). The TCXO uses a conventional analog thermistor network of coarse compensation and a CMOS digital fine correction systems with a programmable memory for fine compensation. A computer data interpolation method is used to minimize the required number of data points for fine correction.

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Section 1

Purpose

The purpose of this program is to modify the previous development of the high stability temperature compensated crystal oscillator (HSTCXO) initially developed under contract DAAB07-71-C-0136 and DAAB07-73-C-0137. This HSTCXO is digitally compensated and is intended for use as a reference frequency source in advanced tactical communications systems. The program is to include changes in frequency, reduction in power, additional CMOS output, and a wider temperature range. Five advanced exploratory models of the digitally compensated HSTCXO are to be delivered.

Listed below are the objectives of this study, as described in the Technical Guidelines, dated 30 August 1974, authored by the Frequency Control and Signal Processing Devices Technical Area of the Electronics Technology and Devices Laboratory, United States Army Electronics Command (ECOM).

1.1 PERFORMANCE OBJECTIVES

Nominal output frequency	4.5 MHz
Frequency-temperature stability (steady state)	±5 pp 10^8 from -46 to +85 °C
Frequency-temperature stability (retrace)	The frequency change resulting from thermally induced hysteresis shall not exceed ±3 x 10^{-8} at temperatures of -46, +30 and +85 °C when subjected to the following temperature cycle: -57 °C to -46 °C to +30 °C to 85 °C to -46 °C to 85 °C to +30 °C. The HSTCXO shall be maintained at a storage temperature of -57 °C for a minimum of 16 hours preceding the test, and frequency shall be recorded following a 1-1/2-hour stabilization period at each temperature. The maximum time permitted for any one temperature change shall be 1 hour.
Frequency-temperature stability (transient)	±5 pp 10^8 for a ramp 10 °C amplitude, 1 °C/minute ramp starting at -40, -5, +30, and +65 °C stabilized temperatures respectively
Frequency-voltage stability	±5 pp 10^9 (+10 ±0.5 V dc)
Frequency-load stability	±5 pp 10^9 (output A, 50 +5 ohms; output B, 30 ±5 pF)

Frequency adjustment range .... ±1 ppm, minimum

Output voltage

Output A .....0.125 V rms, minimum, in 50 ohms

Output B .....Square wave, 10-volt CMOS compatible, 30 pF

Input power .....10 V ±0.5 V, 10 mA max; output A, 50 ohms; output B, 30 pF

Warmup.....Within ±1 pp 10^8 of final frequency in 1 minute

Spectral purity.....Nonharmonic discrete; spurious shall be 100 dB or more below carrier

1.2 MECHANICAL CHARACTERISTICS

Size.....2.75 x 1.5 x 0.5 inches

1.3 CHANGES

The following areas are to be changed, and the results shall be incorporated into the five advance exploratory models.

a. Frequency changed to 4.5 MHz.
b. Stability with voltage and load.
c. Continue crystal hysteresis study.
d. Add a second output CMOS compatible.
e. Reduce power by use of CMOS devices.
f. Widen the temperature range, keeping the same temperature stability.

Temperature-compensated crystal oscillators with stabilities of ±5 pp 10^7 from -40 to +70 °C have been a commercial realization for about a decade.[1] Such units have been produced by the thousands at reasonable costs. Over 40,000 units have been produced at Collins alone.

A search of tcxo literature reveals that several methods of frequency modulation have been used,[2] but the most common method has been to use a voltage-variable capacitor, or varactor, in series with the crystal. Bias for the varactor is usually supplied from a temperature-sensitive voltage divider that contains two or three thermistors and selected resistors. Stabilities of 1 to 2 pp 10^7 have been achieved in small quantities over the -40 to +70 °C/80 °C temperature range,[3 4] and stabilities of 5 pp 10^8 have also been achieved over narrower ranges in quite small quantities.[4 5 6] In general, it appears that compensation becomes increasingly difficult beyond ±5 pp 10^7 due to the very small component tolerances involved, the interaction of network adjustments, and an undefined degree of electrical hysteresis in crystals due to thermal cycling.

Partial solutions to these limitations, although not entirely desirable from a production standpoint, have been to use a digital computer to solve network calculations, or to use analog "segmented" networks to provide more independence of adjustments. Often a large number of temperature runs have been required to bring units into the 1 to 2 pp 10^7 stability region. For the computerized approach, this is due to lack of accurate component data and the inability to install the exact component values calculated. For the analog segmented approaches, the major difficulty remains the lack of true independence between segments; in addition, a large number of components are required, many of which must be selected to fit each oscillator.

It was evident that production of 5 pp 10^8 tcxo's in large quantities required new and/or improved techniques of compensation. It further was apparent that achieving the required 350:1 reduction in tc would be difficult in one step. This study was based on the concept of using a conventional voltage divider network for coarse compensation and a new digital network for fine compensation. The latter network was conceived, designed, and proven at Collins Radio Company in 1970 and early 1971, using transistor-to-transistor logic (TTL) hardware. A part of previous HSTCXO development has been to package much of the digital circuitry in a custom integrated circuit, thereby reducing the size and cost of digital compensation.

Carried to extremes, digital compensation networks can be expanded to provide stabilities of any desired degree, with or without initial coarse compensation. Ultimate limiting factors are cost, size, and the lack of oscillator components with temperature characteristics that retrace exactly regardless of thermal histories. Crystals and certain capacitors are probably the greatest contributors to retrace errors and have been studied during the course of the HSTCXO development.

In 1971-1972, a high stability temperature compensated crystal oscillator (HSTCXO) was developed under USAEC contract DAAB07-71-C-0136. This unit achieved frequency stabilities of ±5 pp 10^8 from -40 to +80 °C by incorporating two-step compensation; that is, a three-thermistor voltage divider network for coarse compensation to approximately ±4 pp 10^7 and a digital memory for fine correction to ±5 pp 10^8 or less. Except for a custom-designed MOS integrated circuit, models produced on the previous contract used discrete, commercially available components; overall package volume was 6.5 cubic inches.

As reported earlier,[7] the feasibility of a ±5 pp 10^8 stability HSTCXO was established; but there are several real or potential problem areas left that require investigation and solution in order for the HSTCXO to be considered practical for military equipments. These problem areas are thermally induced hysteresis, response to thermal transients, frequency aging, excessive compensation time, and large size.

Thermal nonrepeatability of frequency-temperature data now prevents the verification of ±5 pp 10^8 stability from -40 to +80 °C unless tests are conducted under a given set of conditions not likely to be found in actual applications. The special test conditions prescribe a temperature-time profile that includes a preliminary 10-hour soak of the HSTCXO at room temperature to relax thermal stresses that have been induced at low temperature. Thermal transients must not degrade the fixed-temperature stability significantly if a true ±5 pp 10^8 stability is to be maintained under practical applications, which often include a change of at least 1 °C/minute during transmit cycles. Circuit contribution to frequency aging must be reduced to an insignificant level so it will not add to crystal aging and preclude a reasonable prediction of long-term performance. Simplification of the compensation procedure is also desirable to reduce compensation time and to remove associated excessive costs.

Temperature compensation of crystal oscillators using varactor diodes requires circuitry with memory. That is, the tcxo is like a servo that must operate open-loop because there is no reference signal available more stable than the oscillator being controlled. In the past, memories in tcxo's have been the analog type, incorporating a stable supply voltage and a temperature-sensitive voltage divider of some form. Successful compensation has been based on the supposition that all rf components in the oscillator behave exactly the same from one temperature run to the next and that the analog memory, once adjusted, remembers the continuous stream of correction voltages required for compensation.

Progress in microelectronics now makes possible digital memories that are practical in cost and size for high-stability tcxo's. The analog memory is still cheaper and smaller for rough compensation tasks, but a digital memory offers the distinct advantage of adjustment flexibility, making multiordered correction characteristics and, therefore, high stabilities practical.

A block diagram of the HSTCXO is shown in figure 3-1. Compensation is achieved with both analog and digital memories. The analog, or coarse, memory is used in a conventional manner to reduce the oscillator temperature coefficient (tc) to ±4 pp 10^7 or less; then the digital network adds fine corrections to reduce the overall tc to less than ±5 pp 10^8. Note in the block diagram that the digital memory is a programmable read-only memory (PROM) that can be programmed to generate digital correction words in response to being addressed by temperature data in a digitized format. Correction words are converted to analog voltage and used to make fine frequency corrections.

The general approach of the development was to carefully apply and refine a combination of existing techniques. Development effort can be generalized into the four areas defined in the following paragraphs.

3.1 COARSE TCXO

Tcxo's with analog compensation have previously been studied in detail (see references 2 and 6, for example) and have needed only minor design refinements. Primarily, these were improved voltage and load coefficients and reduction in power dissipation.

3.2 DIGITAL COMPENSATION NETWORK

Although digital compensation had been achieved previously with TTL hardware, the hardware had to be reduced in size, cost, and power dissipation. This was done by use of CMOS integrated circuits for all the logic circuits. The only TTL hardware was the PROM, for no CMOS PROM was available.

Compensation procedures had to be improved and delineated, and test fixtures that would speed the compensation procedure were developed.

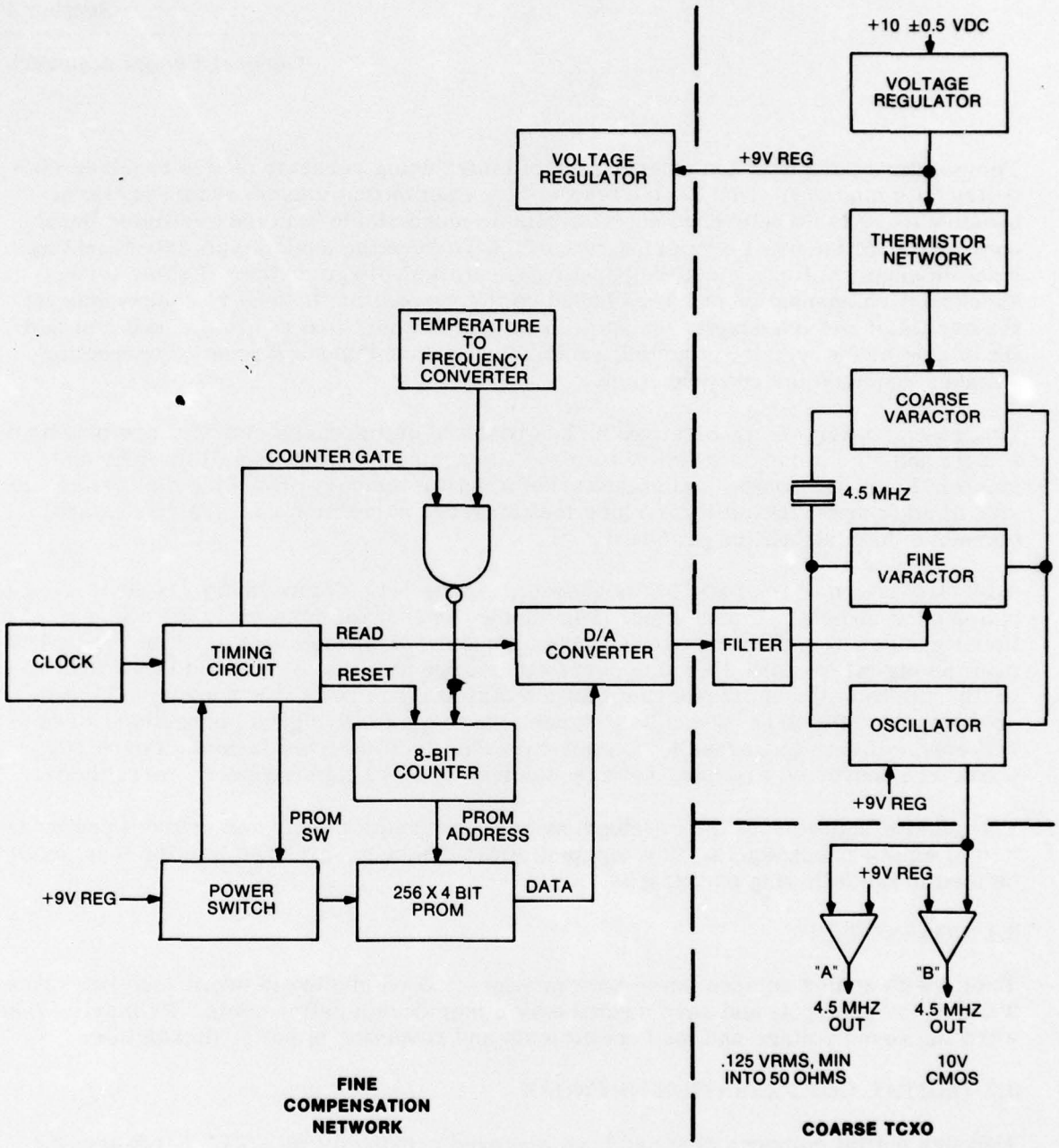


Figure 3-1. High Stability Temperature Compensated Crystal Oscillator (HSTCXO), Block Diagram.

3.3 PACKAGING

Packaging effort was the same as the 5-MHz HSTCXO's built under and included use of thin-film packs for both the digital (contract DAAB07-73-C-0137) and coarse oscillator circuit. Fitting all the additional circuitry into 2 cubic inches was a difficult problem but was completed.

3.4 FREQUENCY RETRACE

The failure of component parameters to retrace at any given temperature, despite varied or even identical histories, can render the compensation of an HSTCXO difficult, if not meaningless. While USAEC did not specifically call for elimination of this effect in its specification guidelines, it did require demonstration of compliance in the presence of the effect.

From the outset, crystals were suspected as a major source of retrace errors. Figure 3-2 shows the retrace error record for a 4-MHz tcxo in 1968. Both frequency-temperature curves were recorded as temperature increased from -55 to +105 °C at 1/2 °C per minute; but curve A followed a 12-hour storage at room temperature, whereas curve B was recorded after storage for 1/2 hour at +105 °C. Note that the error is largest (6.7 pp 10^7) at -55 °C and diminishes as temperature increases. Attempts to prove significant connections between retrace and humidity or stability of other oscillator components proved futile. Finally, the crystal was tested separately and was found to exhibit retrace errors similar to those measured in the tcxo.

With this background knowledge as a start, the HSTCXO study sought to learn more about crystal retrace in order to establish test procedures that would permit compensation and customer verification of ±5 pp 10^8 stability from -46 to +86 °C.

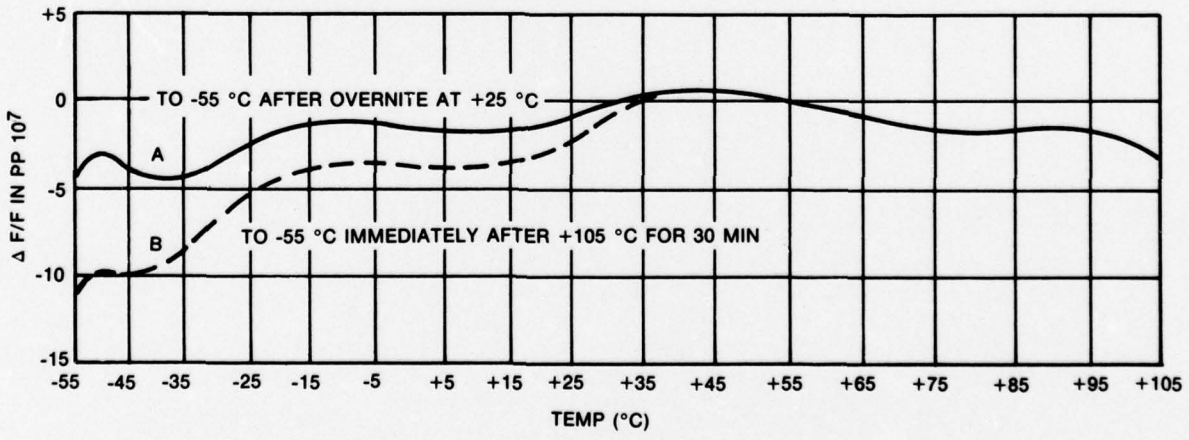


Figure 3-2. Hysteresis Effects in the Frequency-Temperature Characteristics of 4-MHz TCXO (SN8/52).

A schematic diagram of the coarse portion of the HSTCXO is shown in figure 4-1.

4.1 OSCILLATOR/AMPLIFIERS

The rf circuit shown in figure 4-1 is a modified Pierce oscillator followed by one common-base amplifier and a Motorola MC-1550 linear amplifier IC. Stages are stacked in pairs to save power. The emitter resistor of Q3 sets emitter current for both Q2 and Q3, and the current drain of the MC-1550 is also the emitter current of Q9. Power consumption by Q2 and Q3 stages is about 4.5 mW from the 9-volt regulated source. Q9 and U2 stages require nominally about 12 mW from the 10-volt supply, though actual figures depend on the specific MC-1550 used.

The MC-1550 circuit is shown in figure 4-2. It is intended to be used in a common-emitter, common-base cascode configuration (Q_A and Q_B) with Q_C acting as an AGC transistor.

Although the input admittance and the forward transfer admittance are essentially those of a common-emitter transistor, the reverse transfer admittance is about 2 orders of magnitude smaller than a single transistor (less than 0.001 milliohm); hence, the cascode circuit provides extremely good isolation between the load and the oscillator stage. (Small coupling capacitors between stages provide additional isolation.) Using Motorola derivations,[8] the approximate supply current (0.95 mA) was computed by the formula

$$I = (0.31\ V_{cc} - 0.23)\ mA$$

although chip-to-chip variations in element values cause measured and computed values to differ.

Voltage and load coefficients measured less than 5 pp 10^9, even though the +10-V dc tolerance is ±0.5 V instead of ±0.05 V. Formerly Q9 and U2 were biased from +10 V, whereas now they operate from the 9-V regulated line. Thus frequency changes due to reflected load changes from U2/Q9 as voltage is changed should be reduced.

Separate varactors, shown in figure 4-12, are used for coarse (C104) and fine (C105) compensation so that the size of fine correction steps can be held nearly the same at all temperatures. Although coarse compensation voltages could be applied to the cathode and fine voltages to the anode of a single varactor, step sizes would differ by about 2:1 at the two turning points of the crystal. Such variation is undesired since fine step sizes, if determined to be $\leq$ 5 pp 10^8 at room temperature, would exceed the ±5 pp 10^8 spec limit at the lower turning point; and at the upper turning point, the step sizes would be so small that sufficient total range would not be available to correct the coarse tcxo.

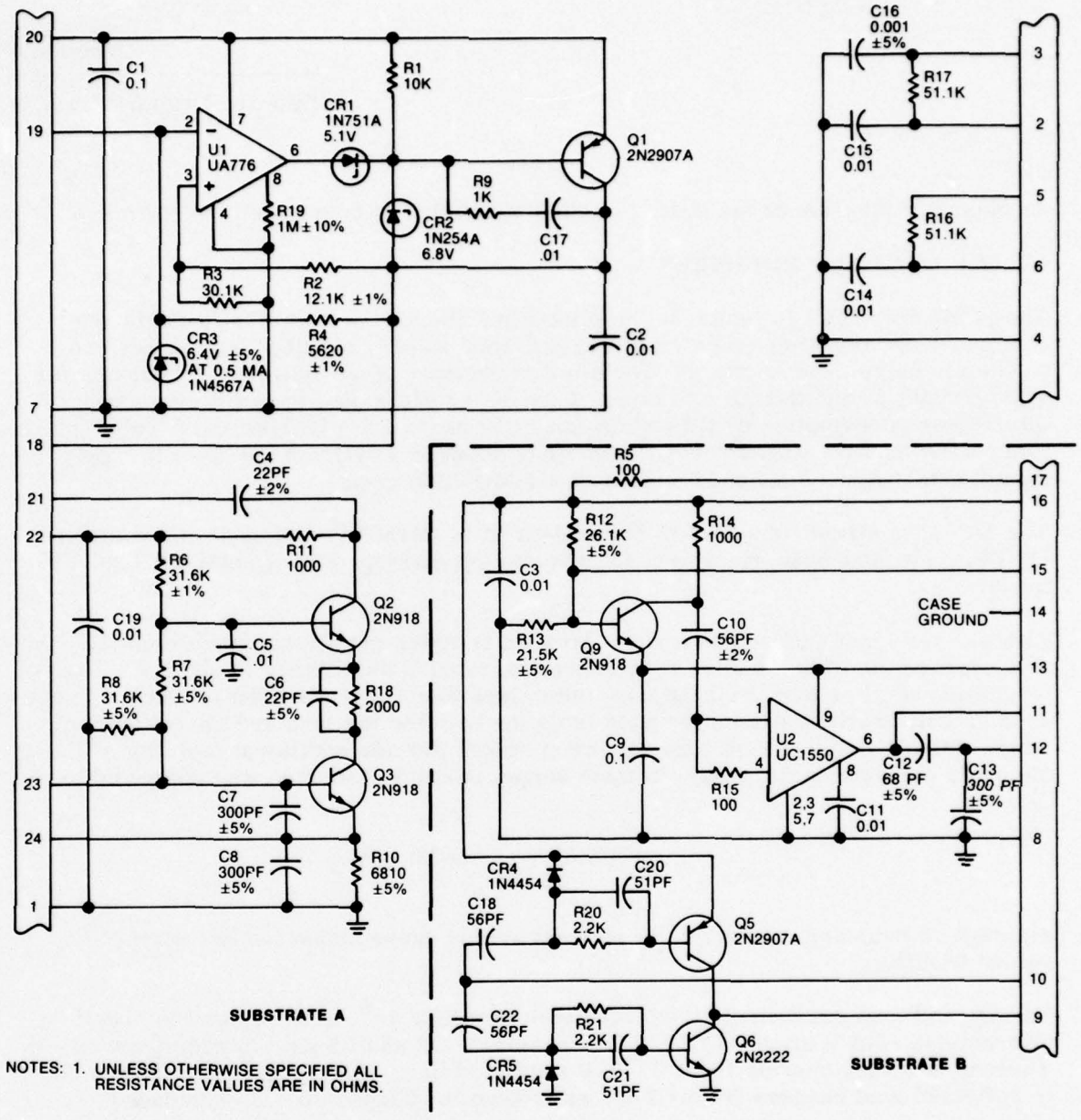


Figure 4-1. Coarse Compensation HSTCXO, Schematic Diagram.

The additional rf output required is a square-wave signal compatible with complementary MOS logic operating at +10 V dc. That is, the low level must be between 0 and +1 V dc, and the high level must be between +9 and +10 V dc. The amplifier circuit shown in figure 4-3 must therefore be added to the oscillator/amplifier thin-film substrate. This high-speed complementary switch provides a symmetrical square-wave signal into a 30-pF load and requires approximately 20 mW of power from the +10-V dc supply.

Inspection of the layout, figure 4-17, shows that these parts were added to the oscillator/amplifier substrate by replacing some large thin-film resistors with chip resistors and by rearranging parts. New tooling was required for the new layout.

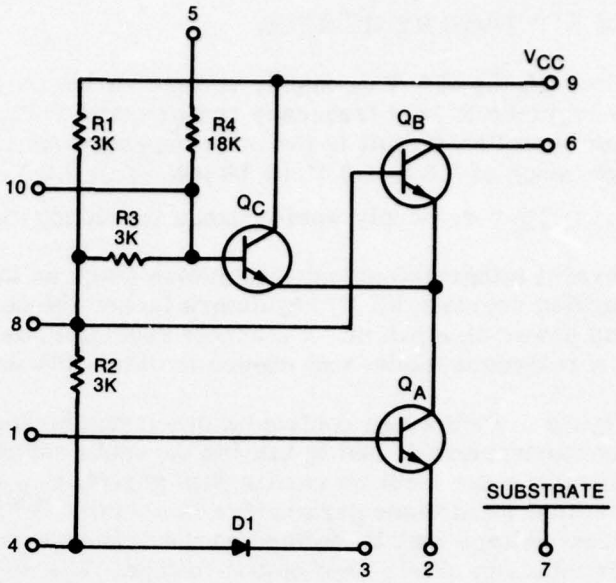


Figure 4-2. Motorola MC-1550 Amplifier Integrated Circuit, Schematic Diagram.

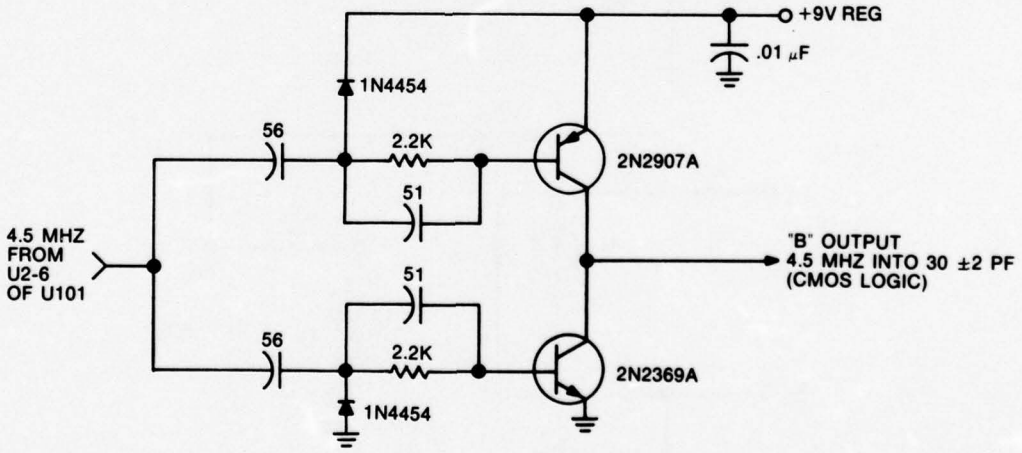


Figure 4-3. Square-Wave CMOS Output Amplifier, Schematic Diagram.

4.2 VOLTAGE REGULATOR

Although the +10-V dc supply voltage varies only ±0.5 V dc, further voltage regulation is required to hold frequency changes with voltage to less than ±5 pp 10^9. The coarse compensation circuit is the most dependent on voltage -- 35 ppm for a varactor voltage range of 0.5 to 4.0 V, or 10 ppm/V at 2.0 V dc. Without regulation, a 0.5-V change in the 10-V dc supply would change frequency about 0.5 V x $\frac{2.0\ \text{V}}{10.0\ \text{V}}$ x $\frac{10\ \text{ppm}}{\text{V}}$, or 1.0 ppm.

Several integrated circuit regulators (such as the Fairchild μA723) were considered. In varying degrees, all IC regulators lacked the desired control of temperature stability and power dissipation. A discrete regulator, using an operational amplifier and a 0.5-mA reference diode, was chosen to obtain the required control.

Figure 4-4 shows an equivalent dc circuit for an operational amplifier (opamp). Current generators I_1 and I_2 are the currents out of the two input terminals, as usually given in some form on vendor data sheets; E_{os} is the input-offset voltage. (Usually the inverse of these parameters is actually defined on data sheets. That is, input-offset voltage may be defined as the voltage that must be applied between the input terminals to obtain zero output voltage. E_{os} appears because of inadvertent differences in bias of input stages, so the polarity may be positive or negative.)

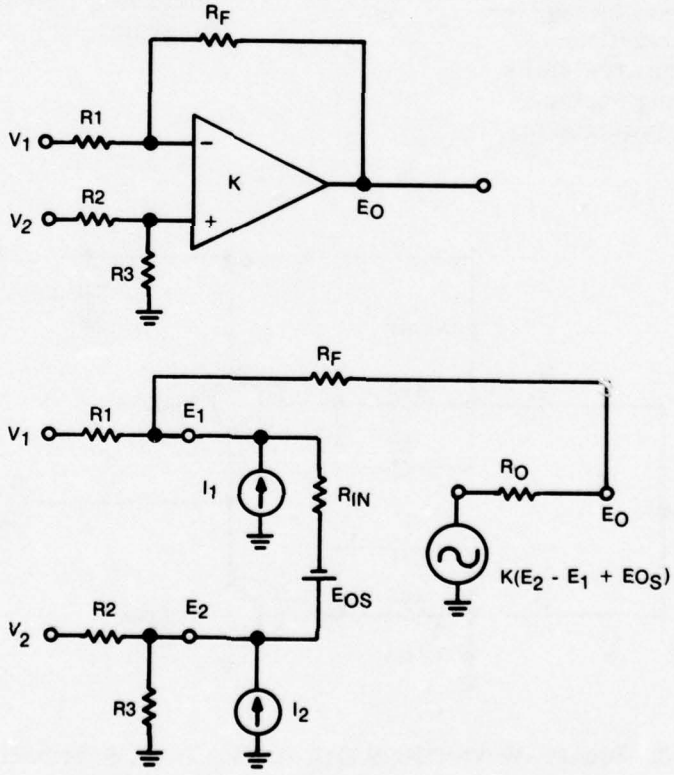


Figure 4-4. DC Model for an Operational Amplifier, Schematic Diagram.

Assuming R_{IN} is very high and R_O is very low, a formula for computing output voltage can be derived by first finding E_2 and E_1:

$$E_2 = \frac{R_3}{R_2 + R_3} \cdot V_2 + \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot I_2$$

$$E_1 = \frac{R_f}{R_1 + R_f} \cdot V_1 + \frac{R_1 \cdot R_f}{R_1 + R_f} \cdot I_1 + \frac{R_1}{R_1 + R_f} \cdot E_o$$

Then,

$$E_o = K (E_2 - E_1 + E_{os})$$

After reduction we have

$$E_O = \frac{1}{(\frac{1}{K} + \frac{R_1}{R_1 + R_f})} \cdot \left[E_{os} + \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot I_2 - \frac{R_1 \cdot R_f}{R_1 + R_f} \cdot I_1 + \frac{R_3}{R_2 + R_3} \cdot V_2 - \frac{R_f}{R_1 + R_f} \cdot V_1 \right]$$

If the open-loop gain, K, is assumed very high, and E_{os}, I_1, and I_2 are assumed very low, the output voltage formula is simplified to

$$E_o = (1 + \frac{R_f}{R_1}) (\frac{R_3}{R_2 + R_3} \cdot V_2 - \frac{R_f}{R_1 + R_f} \cdot V_1)$$

This equation was used to calculate resistor values for a simple 7-V dc regulator, shown in figure 4-5. Output voltages measured in a breadboarded circuit were within tolerances at room temperature, and all three opamp samples tested could supply the 4-mA target load current at 7.0 V dc. At -40 °C, however, there was a large variation in current that could be supplied at 7 V dc (2.2 to 15 mA). At first it was suspected that E_{os}, I_1, and I_2 might not be negligible as first assumed. Using maximum data sheet values for calculations, however, one finds that output voltage should increase at low temperatures and should increase only about 10 mV at -55 °C. The actual limitation on output current not well spelled out on the μA741 data sheet, but the minimum output voltage swing of ±10 V into a 2-kilohm load with a ±15-V supply scales down to something like 3.3 mA for a 10-V supply. Obviously the real cause for poor load regulation is the output current limitation in the μA741 output stage.

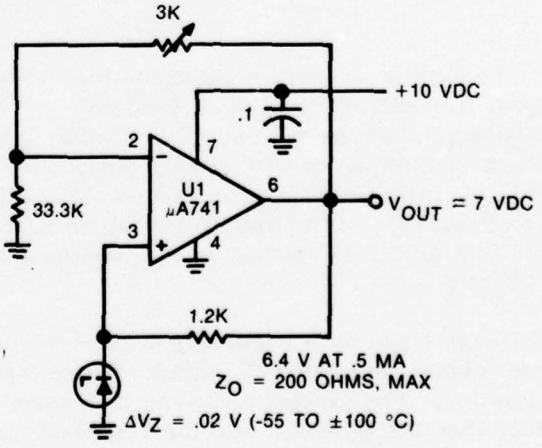


Figure 4-5. 7-Volt Voltage Regulator, Schematic Diagram.

The solution called for an external pass transistor. An npn could be used as an emitter follower, but output voltage would then be another diode drop less than the opamp output level. Since the regulator output should be as high as possible for the coarse compensation network, a pnp transistor was used in a 9-V dc regulator circuit shown in figure 4-1 and duplicated in figure 4-6. Zener diode CR1 is required to permit the opamp output to run in the middle of its range. Diode CR2 is needed to start the regulator; when power is first applied, E_{os} is amplified with open loop gain, and the opamp saturates at maximum output. If CR2 were not present to cause CR1 to conduct, Q1 would stay off, and output voltage would remain at zero. In normal operation, CR2 is reverse-biased with less than 1 V dc; at this bias level, the leakage resistance is very high. Either a μA741 or a μA776 opamp could be used, but the μA776 is a low-power device requiring only 0.2-mA nominal standby current with the value shown for set resistor R19. In comparison, the μA741 requires about 0.5 mA and cannot be varied.

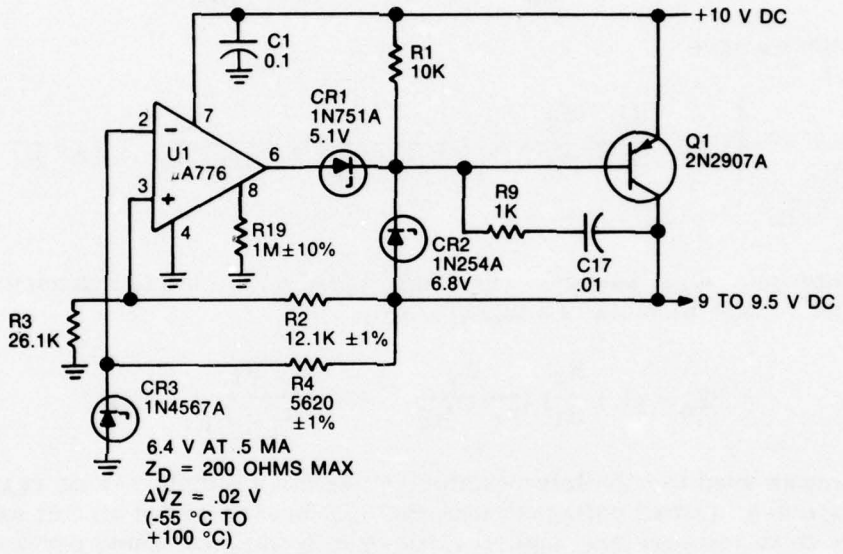


Figure 4-6. 9-Volt Voltage Regulator, Schematic Diagram.

Line regulation is very good since the reference diode is biased from the regulated output; in addition, total open loop gain is the product of the gains of Q1 and U1. Output voltage changes with supply voltage, however, due to the change in input-offset voltage in the opamp with supply voltage. For the μA776, the maximum supply voltage rejection ratio, E_{os}/V_{cc}, is 200 μV/V. Substituting 0.2 kΩ, 5.7 kΩ, 7.4 V, 12.1 kΩ, 26.1 kΩ, and E_o in the opamp model for R_1, R_f, V_1, R_3, R_2, and V_2, respectively, one finds that a 200-μV change in E_{os} due to a 1-volt change in supply will affect the output by about 0.3 mV.

Results of tests on a regulator with two types of amplifiers are shown in table 4-1, and a continuous recording of output voltage, as supply voltage was varied, is shown in figure 4-7. The circuit requires less than 1 mA if the μA776 is used; line regulation is better than 0.1 percent; and the required input-output voltage differential is less than 100 mV (compared to typically 3 V for IC regulators).

Table 4-1. Performance Data for 9-V DC Regulators.

SAMPLE	TEMPERATURE (°C)	INPUT CURRENT FOR 4-mA LOAD WITH 10-V INPUT (mA)	OUTPUT VOLTAGE (V DC)							
			INTO 4-mA LOAD WITH INPUT VOLTAGES				FOR INPUT VOLTAGE = 10 V DC AND FOR LOAD CURRENTS			
			9.0 V	9.5 V	10.0 V	10.5 V	1.0 mA	5 mA	10 mA	20 mA
No 1 μA776	+30	4.95	8.9462	9.0016	9.0009	9.0011	9.0017	9.0003	8.9991	7.4065
	+100	4.95	8.9424	9.0009	9.0010	9.0007	9.0018	9.0003	8.9986	8.9946
	-55	5.0	8.9664	9.0014	9.0015	9.0014	9.0024	9.0013	8.9992	8.9955
No 2 μA741	+30	5.5	8.9082	9.0040	9.0036	9.0031	9.0012	9.0001	8.9985	8.9949
	+100	5.4	8.9194	9.0021	9.0020	9.0017	9.0045	9.0028	9.0011	8.9973
	-55	5.6	8.9533	9.0005	9.0006	9.0006	9.0016	9.0002	8.9986	9.0002

NOTES: 1N4567A reference diodes were not available at time of test; an uncompensated 1N753 zener uas used, and R1 was adjusted to set output voltage to 9 V dc nominal at each temperature.

Voltage test instrument was an HP 2401C digital voltmeter.

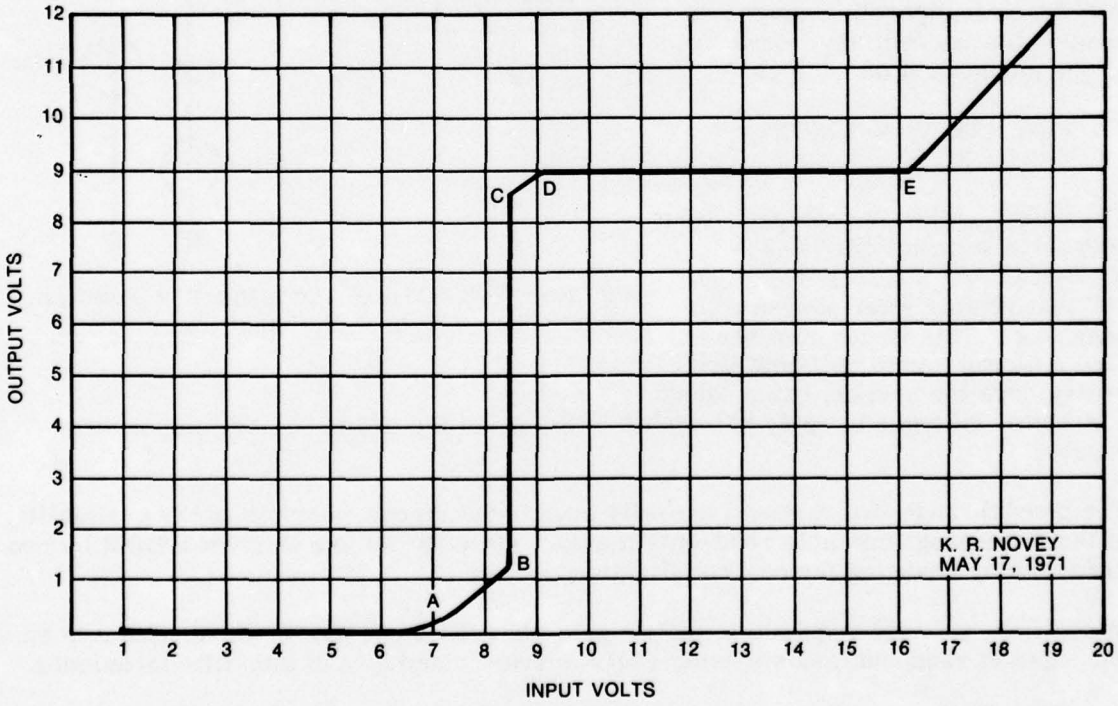


Figure 4-7. 9-Volt Voltage Regulator Output Vs Input Voltage With 4-mA Load.

As expected, frequency variations with supply voltage were almost nil when measured on completed HSTCXO models. Results are summarized in section 6. Better voltage coefficients have been realized because the two output stages (Q9 and U2) were operated from the 9-V regulated line rather than the 10-V supply. Table 4-1 data shows the regulator can tolerate even a 10-mA load without losing control and, therefore, could supply an additional 1 to 3 mA for Q9 and U2.

The total loop gain being the product of Q1 and U1 can cause a potentially unstable regulator, since this allows gain to exist when the phase shift is 180°. This is eliminated, as seen in figure 4-6, by the use of R9 and C7. The addition of this network reduces the ac gain of the transistor stage, thus increasing the phase margin and allowing stable operation.

4.3 COARSE COMPENSATION NETWORK

A continuous, passive voltage divider network is used as the coarse compensation memory, as shown in figure 4-1 (and redrawn in figure 4-8 for convenience). A number of papers in the literature discuss this circuit (such as reference 6), so little will be added here.

Small variable resistors were first used for R101, R102, and R103, but intermittent wipers forced the selection of two series resistors for each resistive leg. Selected in test, R102 is determined at -46 °C, R101 at +30 °C, and R103 at +85 °C. Successive temperature runs are required to correct any interactions of one adjustment on another.

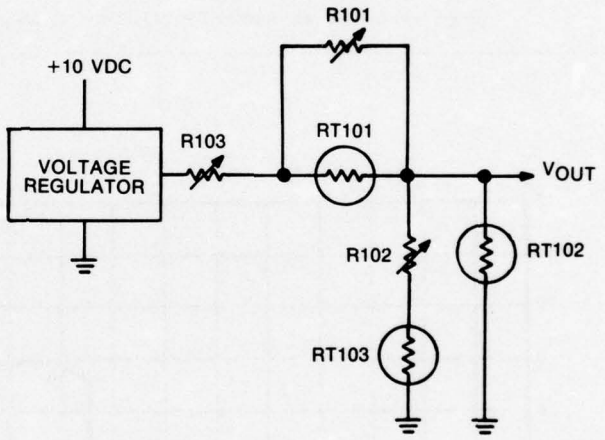


Figure 4-8. Coarse Compensation Network, Schematic Diagram.

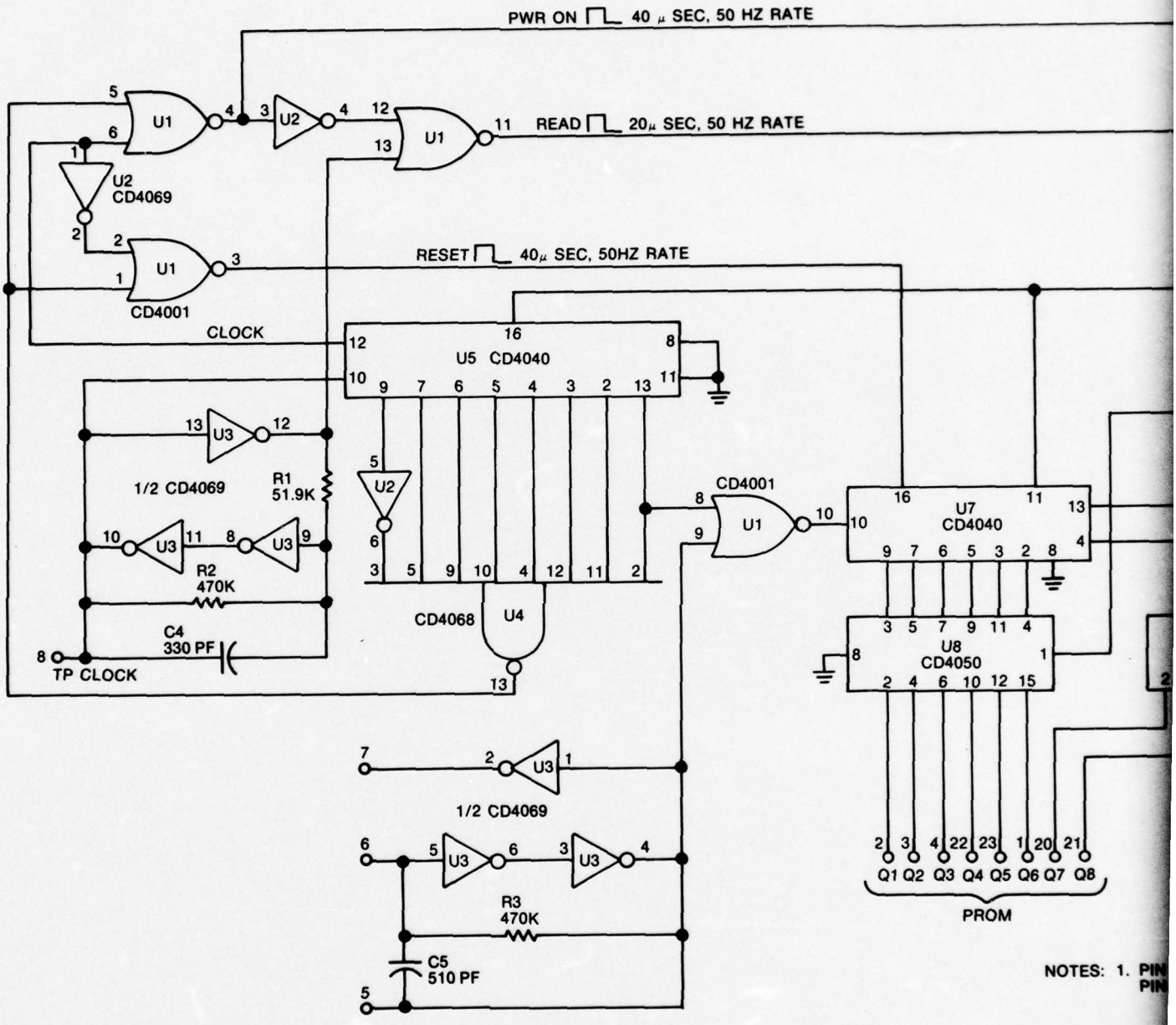
4.4 FINE COMPENSATION NETWORK

The object of the fine compensation network shown in figure 4-9 is to correct errors greater than 5 pp 10^8 that remain after coarse compensation. This is accomplished with a digital memory (U202) that remembers the proper, independent correction voltages to apply at regular intervals in the -46 to +86 °C temperature range.

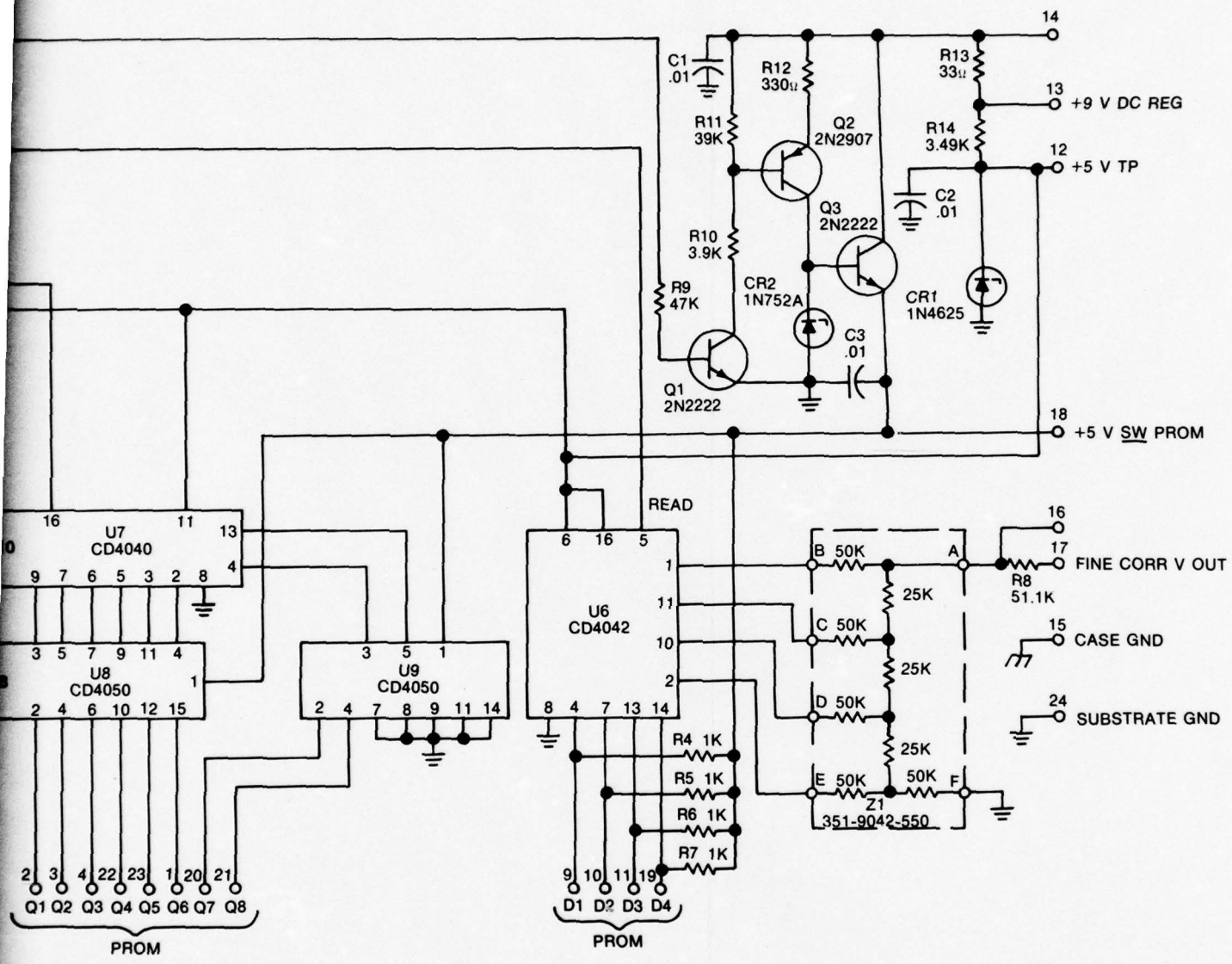
The breakthrough that makes a digitally segmented circuit possible is the availability of the field-programmable read-only memory (PROM); no longer must a ROM be programmed by changing factory metalization masks.

In addition, circuits required to interrogate the PROM can now be integrated into small packages at reasonable costs using CMOS circuitry and hybrid thin-film techniques.

The block diagram in figure 4-10 shows how the PROM is used for digital compensation. Briefly, the PROM is addressed by the states of digital dividers that count the frequency of a temperature-sensitive oscillator; then a ladder network converts the output



NOTES: 1. PIN
PIN



NOTES: 1. PIN 7 IS GND ON U1, U2, U3, U4
PIN 14 IS +5 V ON U1, U2, U3, U4

Figure 4-9. Digital Compensation Network, Schematic Diagram.

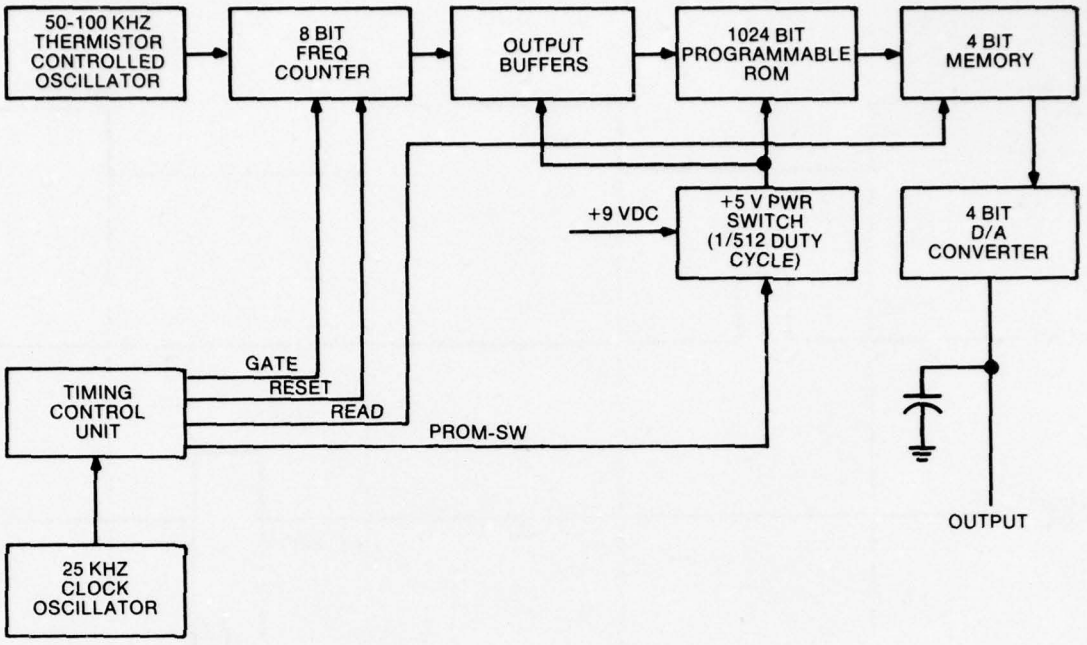


Figure 4-10. Digital Fine Compensation Network, Block Diagram.

words of the programmed ROM to analog voltages for tcxo correction. A clock and associated timing logic provide periodic updates and in general regulate the sequential operation (refer to figure 4-11) of the temperature registers (dividers), power-saving switches, and a temporary memory that holds the ROM output word from one update to another. Required programming for the ROM is determined by stabilizing the tcxo at fixed temperatures, recording the states of temperature registers, and simulating the correct output word with a manual switch. Required programming at intermediate temperatures is computer-interpolated, and the entire ROM is then programmed and installed in the tcxo.

4.4.1 Field-Programmable ROM

In mid-1970, Harris Semiconductors introduced one of the first reliable programmable memories of significant size, the PROM-0512. This TTL memory is organized in a 64 by 8 format, meaning that there are 64 words of memory that are addressable, and each of these words can be programmed with a logic 0 or 1 on each of 8 output lines. Programming, which can be done manually or automatically, is executed by addressing the desired word and applying in current ramp to the output lines on which a logic 1 is desired. The current ramp fuses a nichrome memory element, one of 512, which would have yielded a logic 0 output if not fused. Once programmed, the logic 1's cannot be changed back to 0's. Several semiconductor companies have entered the PROM field since 1970, and a number of TTL and MOS PROM's are now available in a variety of formats and programming methods. Some are even reprogrammable.

The required format is a matter of studied compromise between complexity and accuracy. Too many address (input) words create a data handling and programming problem; too few would mean some steep-sloped errors could escape correction if

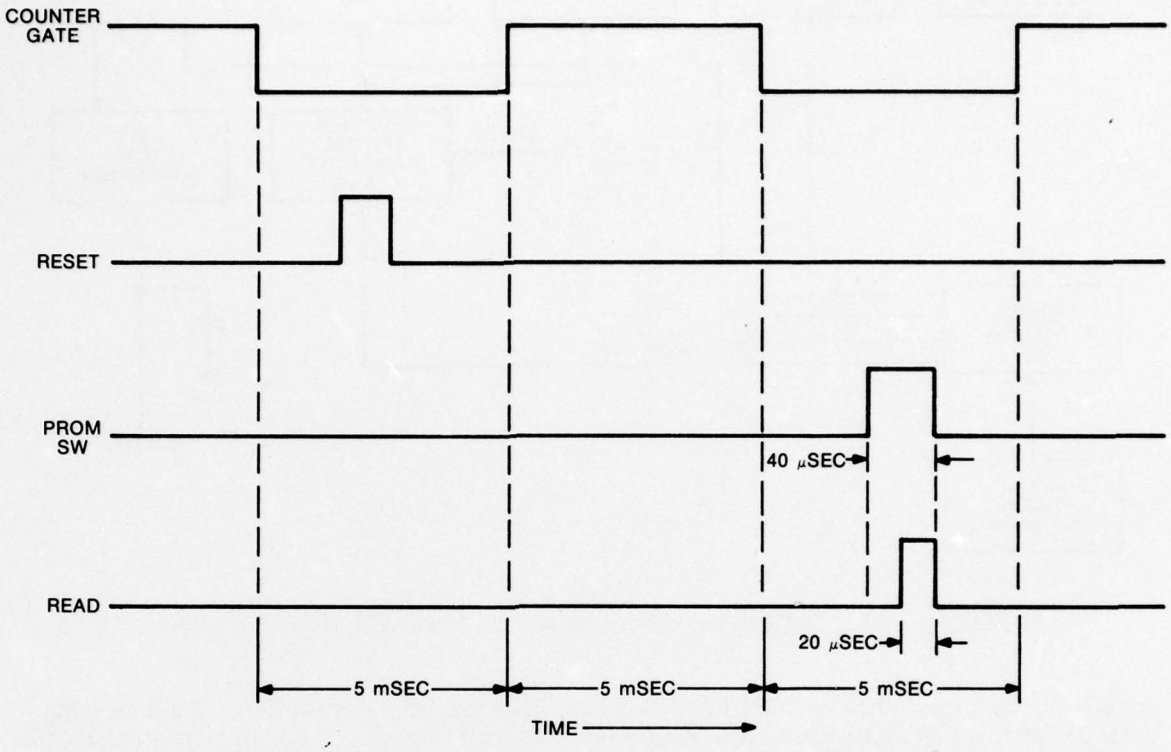


Figure 4-11. Timing Diagram.

they occur between the temperatures used to address the ROM. Also, too many correction (output) words would provide finer voltage increments than necessary; too few would mean insufficient resolution of correction voltage, regardless of the number of address words.

A Monolythic Memories MM5300, with a 256 by 4 format, was chosen for constructing the HSTCXO models. The MM5300 uses fusible nichrome links much like the Harris PROM-0512.

4.4.2 RC Oscillators

U3 in figure 4-9 is an RCA CD4069 hex inverter used to form two RC oscillators that generate input signals for the CMOS dividers and counter. The CD4069 is a complementary MOS circuit (CMOS) chosen for low power dissipation since both oscillators must run continuously.

Requirements for the RC oscillators include good voltage coefficients, good frequency retrace, and a low temperature coefficient for the 25-kHz oscillator. The supply voltage is obtained by biasing U3 from a 0.25-mA zener diode, CR1, which in turn is supplied from the 9-V regulator. Frequency jumps and lack of retrace were exhibited with mica timing capacitors, but retrace was satisfactory with monolythic ceramic capacitors.

To determine the required timing resistance as a function of temperature for the temperature-sensing oscillator, a decade box was extended on leads outside the temperature chamber. A simple network consisting of a 2-kilohm resistor in series with a 10-kilohm positive tc thermistor (Sensistor) fails to match the requirement at -46 °C. A more complicated network was synthesized and used for approximating R_t, using an additional resistor and a 1-megohm negative tc thermistor. Final resistance values for R203 and R202 (shown in the schematic of figure 4-12) were therefore selected by trial and error, and the results appear to justify the larger circuit. The frequency-temperature (F-T) characteristic of the selected circuit is plotted in figure 4-13 along with the measured stability of the 50-kHz oscillator.

The 50- to 100-kHz frequency range is only approximate. A more accurate determination is possible by inspecting the timing and counter circuits of figure 4-10. The address at any temperature is given by the following

$$\text{Address} = 256 \left(\frac{\text{f-temp}}{2\ \text{f clock}} - 1\right)$$

Note that the clock oscillator runs at half the lowest temperature oscillator frequency. This is true only under the conditions of F-T max - F-T min $< 2\ f_c$ to avoid ambiguity of addresses.

In practice, the ROM input address is monitored, not F-T max or F-T min, as the RC oscillators are tuned. Also, in actual practice, it is not necessary that the temperature counter be fully filled once but not more than twice. That is, it can be filled 7/8 to 1-7/8 times, or 1-1/4 to 2-1/4 times, just as long as there is no overlap; usually the ROM address range is set four to seven states short of an overlap by selecting R202. (An overlap would represent an ambiguous determination of temperature.) Selection of R202 is required in each HSTCXO due to parameter variations in oscillator components.

4.4.3 Power Switches

Power dissipation in the digital compensator has been reduced about 90 percent by applying power to such devices as the ROM and the output buffers only when needed.

The power switch operating on a 0.2-percent duty cycle is redrawn in figure 4-14. Note the switch interrupting the +5-V line to the PROM. Note that the +5-V PROM supply is derived from the +9-V supply so that a resistor, R13, and capacitor, C201, can be used to store energy when the ROM is off and thereby reduce the noise conducted to the +9-V supply. Switching the B+ lead to the ROM is necessary because it would dissipate 350 to 500 mW if left on continuously. To prevent the tcxo from losing compensation during the off cycle of the ROM, a low-power memory is left on continuously and is used to retain the last ROM output word until the next update.

4.4.4 4-Bit Memory

U6 in figure 4-9 is a 4-bit latch that reads in and holds the 4-bit output word from the PROM; this is done on command from a read pulse produced in the CMOS timing circuit and occurs about every 20 ms. This temporary memory, which is energized continually, would not be required if the PROM did not have to be operated at a 0.2-percent duty cycle to conserve power. The RCA CD4042AD contains four type D CMOS flip-flops requiring a total power of only about 1 mW. Unlike U1, the supply voltage to U3 is regulated by CR1 and the 9-volt regulator. Isolation from voltage

variations is essential, since analog fine correction voltages are derived from logic 0 and 1 output levels from U6.

4.4.5 D/A Converter

Conversion from 4-bit digital words to 16 equally spaced analog voltages is achieved in Z1. This is an R/2R resistive ladder, where R is 25 kilohms for low power dissipation. Conversion accuracy and tc requirements are easily satisfied with the Sprague UHF-010 ladder.

Selection of resistor R201 shown in the schematic of figure 4-12 determines the total range of output voltage and, therefore, the voltage increment for each of 16 steps.

4.4.6 RC Filter

The d/a converter is followed by an RC filter with a time constant of about 7.5 seconds. Filtering serves two purposes: first, it attenuates the frequency modulation of the carrier at a 49-Hz (1/20.48-ms) update rate of the compensator, and second, it produces a smooth function of compensation voltages rather than 16 abrupt steps. An example of the latter effect can be seen at a temperature where the decimal ROM address is, say, 25 for 25 percent of the time and 26 for the other 75 percent; if the ROM had been programmed to produce analog output voltages of, say, 2.0 and 1.0 V dc at these addresses, the filtered output voltage would be about 1.25 V dc.

Signal-to-noise measurements have been taken and are included in section 6.

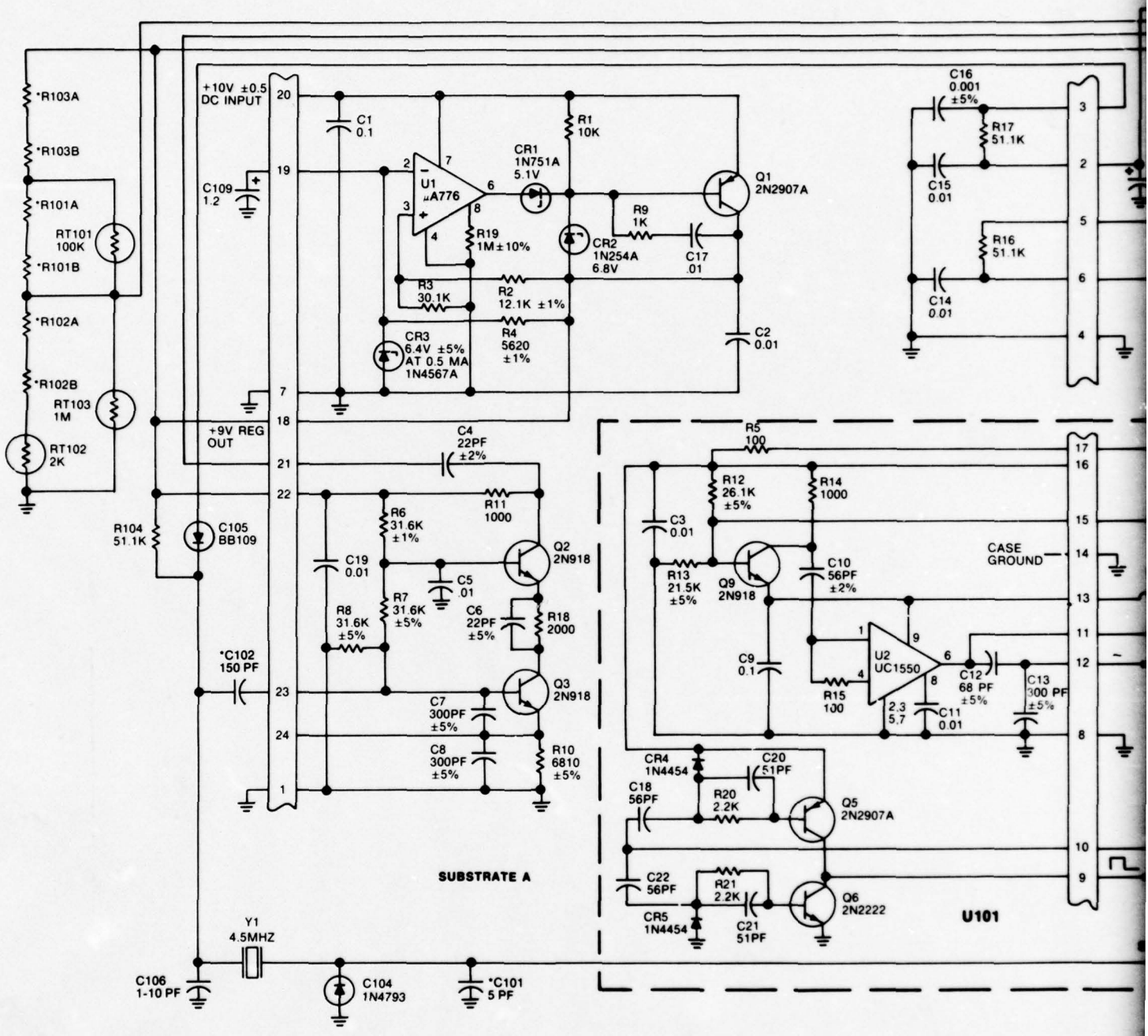
4.5 POWER DISSIPATION

The minimization of power dissipation has been a constant concern, not only to meet the 100-mW specification, but also to minimize warmup drift as discussed in the preceding section. Power switching was used where possible, and low-power devices were selected if available. A summary of the anticipated maximum dissipations for the different HSTCXO elements is shown in table 4-2. Some of the figures are estimates based on vendor data sheets, and others are based on breadboard tests. Power measurements on completed HSTCXO's (section 6) show typical dissipations are in the 65- to 78-mW range.

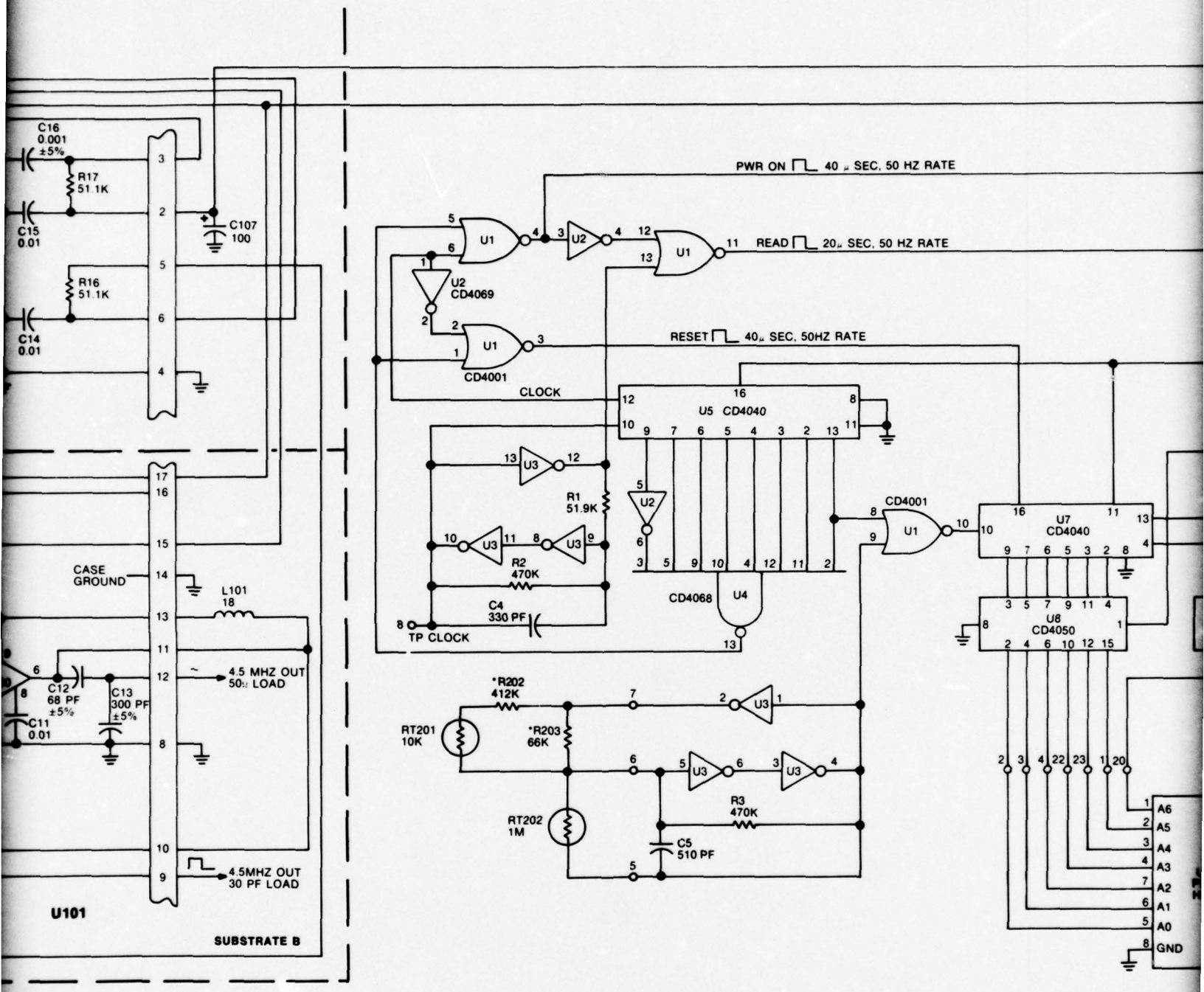
4.6 PACKAGING

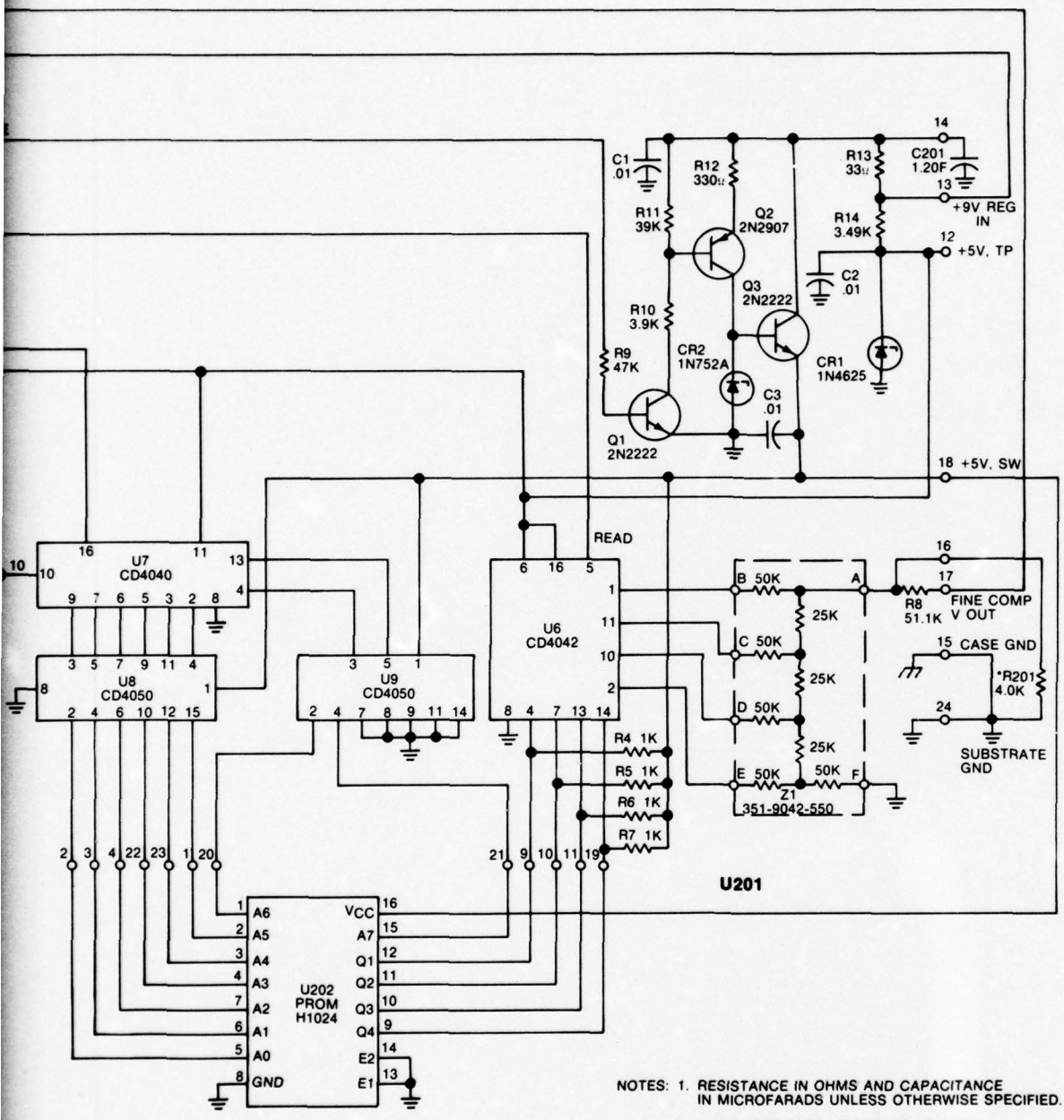
The number, size, and configuration of thin-film packages were major constraints on overall packaging. It was determined that two metal enclosures, figure 4-15, each about 0.2 x 0.75 x 1.25 inches, offered the best volume efficiency of the available packages and could also be hermetically sealed. Figure 4-16 is an outline drawing of this enclosure. Circuitry was partitioned into two functions: the oscillator/amplifier function shown in figure 4-1 and the digital fine compensation circuit shown in figure 4-9. These schematics also show the external components required to complete the coarse and fine compensation functions. There are only two connecting lines between the two circuits (+9 V regulated and fine correction voltage). The overall schematic is shown in figure 4-12. Respective layouts of these two circuits are shown in figures 4-17 through 4-20.

The overall HSTCXO package layout is sketched in figure 4-21 and photos are shown in figures 4-22 and 4-23. Maximum dimensions are 0.5 x 1.5 x 2.75 inches, or 2.0625 cubic inches. There are two compartments: a coarse tcxo and a smaller fine


*R103A
*R103B
*R101A
RT101 100K
*R101B
*R102A
*R102B
RT103 1M
RT102 2K
+10V ±0.5 DC INPUT
+9V REG OUT
C109 1.2
C1 0.1
U1 μA776
CR1 1N751A 5.1V
R1 10K
Q1 2N2907A
R9 1K
CR2 1N254A 6.8V
C17 .01
R19 1M±10%
R3 30.1K
R2 12.1K ±1%
R4 5620 ±1%
CR3 6.4V ±5% AT 0.5 MA 1N4567A
C2 0.01
C16 0.001 ±5%
R17 51.1K
C15 0.01
R16 51.1K
C14 0.01
C4 22PF ±2%
R11 1000
R6 31.6K ±1%
C19 0.01
Q2 2N918
C5 .01
R7 31.6K ±5%
R8 31.6K ±5%
C6 22PF ±5%
R18 2000
*C102 150 PF
Q3 2N918
C7 300PF ±5%
C8 300PF ±5%
R10 6810 ±5%
R104 51.1K
C105 BB109
R5 100
R12 26.1K ±5%
R14 1000
C3 0.01
R13 21.5K ±5%
Q9 2N918
C10 56PF ±2%
CASE GROUND
C9 0.1
U2 UC1550
R15 100
C12 68 PF ±5%
C13 300 PF ±5%
C11 0.01
CR4 1N4454
C20 51PF
C18 56PF
R20 2.2K
Q5 2N2907A
C22 56PF
R21 2.2K
Q6 2N2222
CR5 1N4454
C21 51PF
U101
SUBSTRATE A
Y1 4.5MHZ
C106 1-10 PF
C104 1N4793
*C101 5 PF

2-1


C16
0.001
±5%
R17
51.1K
C15
0.01
R16
51.1K
C14
0.01
C107
100
CASE
GROUND
L101
18
C12
68 PF
±5%
C13
300 PF
±5%
C11
0.01
4.5 MHZ OUT
50Ω LOAD
4.5MHZ OUT
30 PF LOAD
U101
SUBSTRATE B
PWR ON 40 μ SEC. 50 HZ RATE
READ 20μ SEC. 50 HZ RATE
RESET 40μ SEC. 50HZ RATE
U1
U2
U2 CD4069
CD4001
CLOCK
U5 CD4040
U3
R1
51.9K
R2
470K
C4
330 PF
TP CLOCK
CD4068
U4
CD4001
U7
CD4040
U8
CD4050
*R202
412K
RT201
10K
*R203
66K
RT202
1M
R3
470K
C5
510 PF
A6
A5
A4
A3
A2
A1
A0
GND



NOTES: 1. RESISTANCE IN OHMS AND CAPACITANCE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

2. *INDICATES TEST-SELECT COMPONENT.

Figure 4-12. HSTCXO, Schematic Diagram.

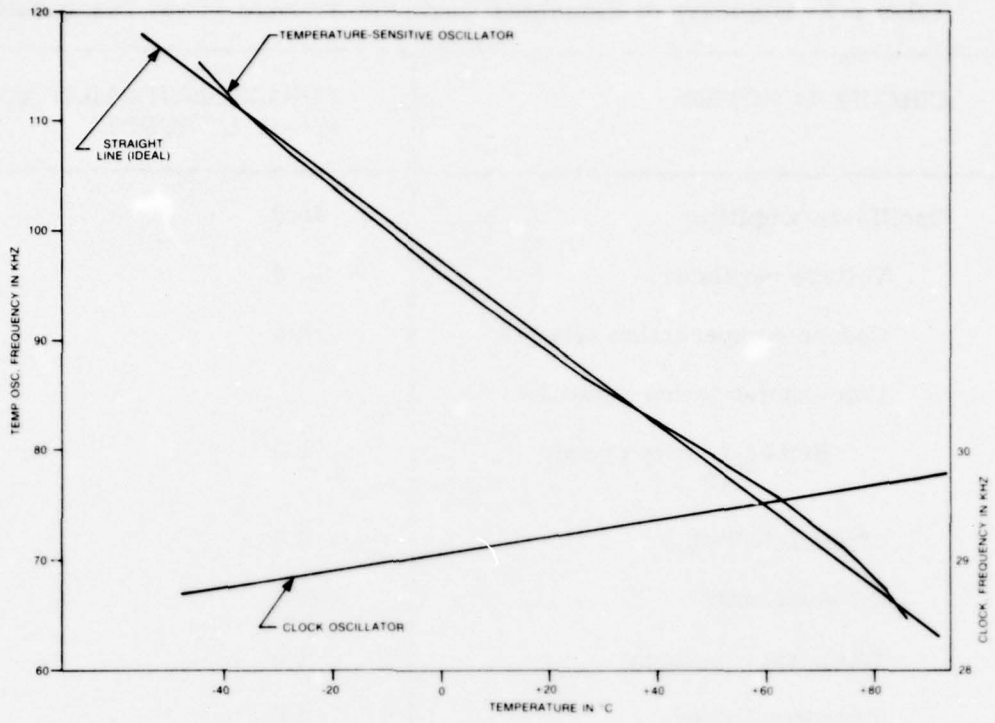


Figure 4-13. F-T Characteristics of RC Oscillators.

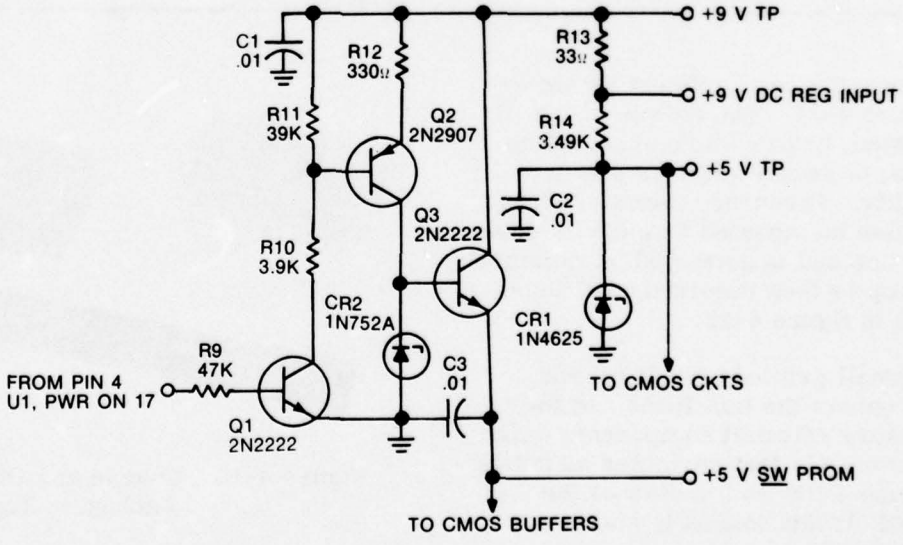


Figure 4-14. Power Switch for PROM and CMOS Buffers.

Table 4-2. Summary of Estimated Maximum Average Power Dissipation.

CIRCUIT FUNCTION	POWER DISSIPATION (mW) +10-VOLT SUPPLY
Oscillator/amplifier	40.0
Voltage regulator	10.0
Coarse compensation network	10.0
Fine compensation network	
ROM ($\frac{1}{512}$ duty cycle)	2.0
CMOS DIGITCXO	0.4
RC oscillators	15.0
Temporary memory	1.0
Resistive ladder	2.0
CMOS output Loaded with 30 pF	20.0
Total	100.4 mW

compensator compartment as shown in figure 4-24. The coarse tcxo will be sealed, before fine compensation begins, to reduce changes due to humidity. Frequency trimmer C106 may also be mounted through the base since one end is grounded; a moisture seal cap is then required on C106 as shown in figure 4-22.

Two small printed circuit boards interconnect the thin films and the necessary external components which are primarily test variables as shown in figure 4-25. A top view of the printed circuit boards is shown in figure 4-24.

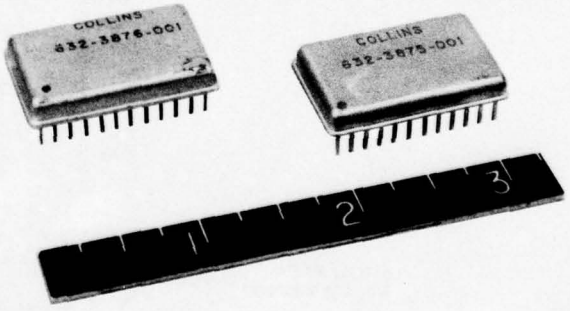


Figure 4-15. Coarse and Digital Packages, Top View.

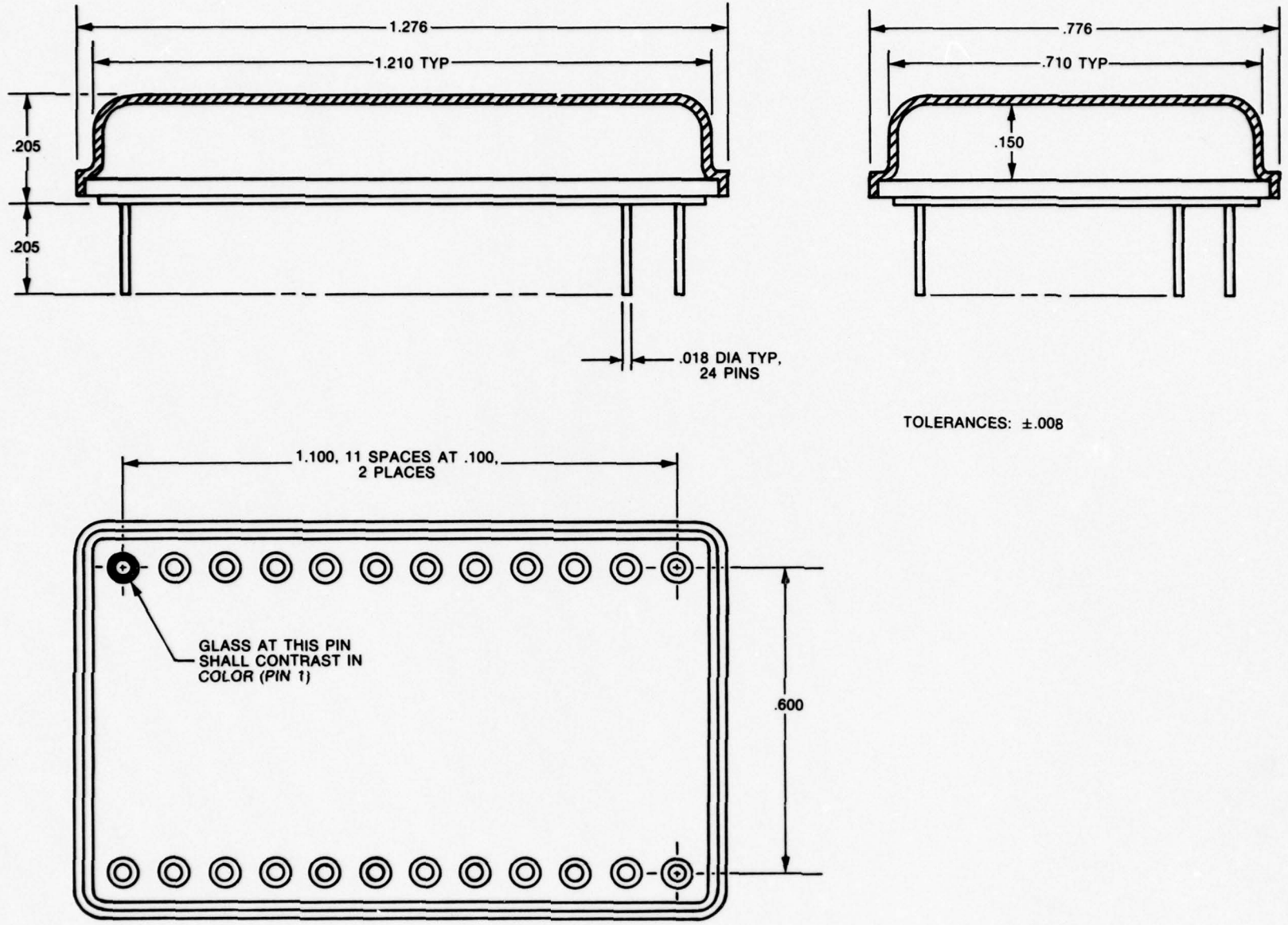
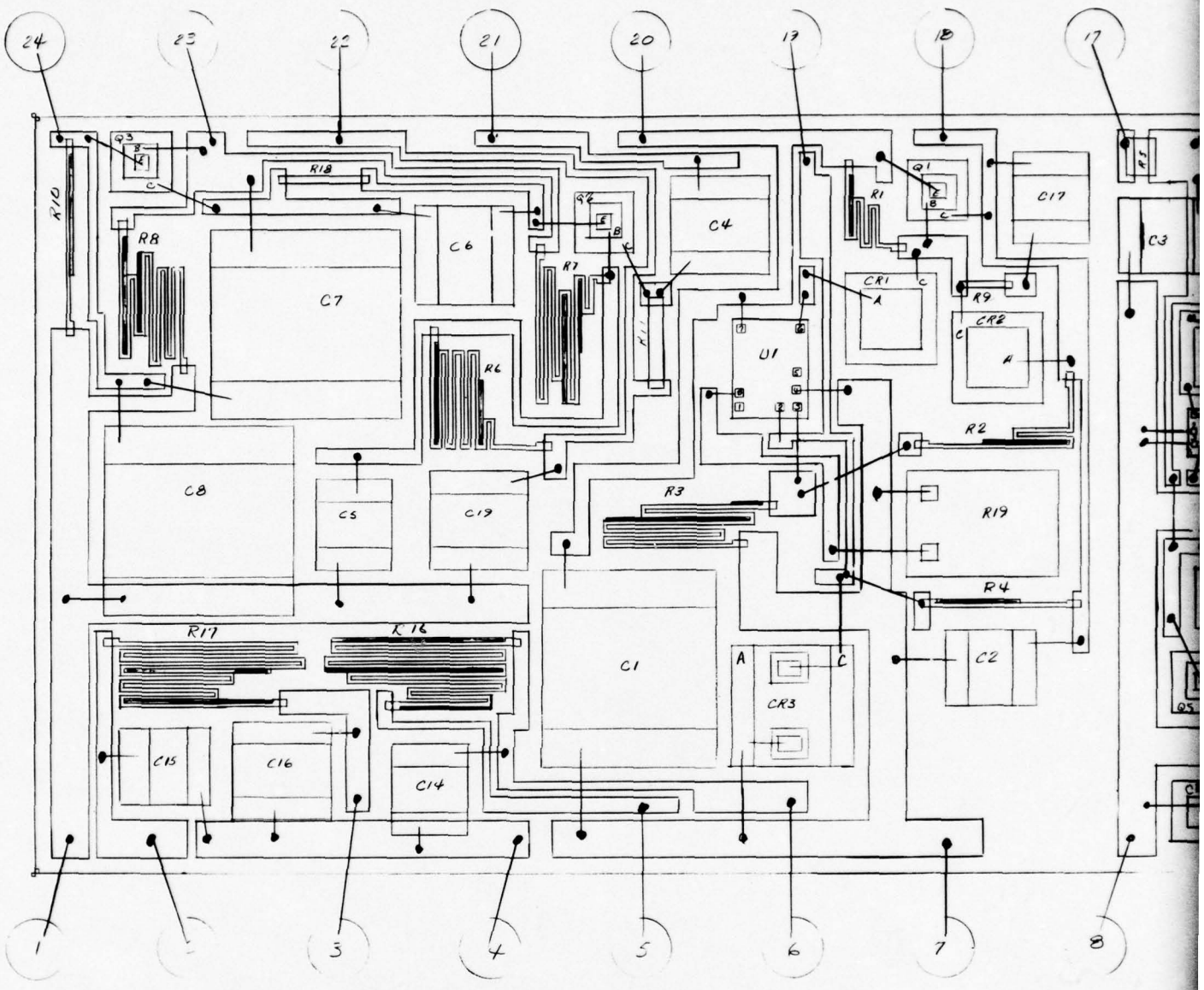
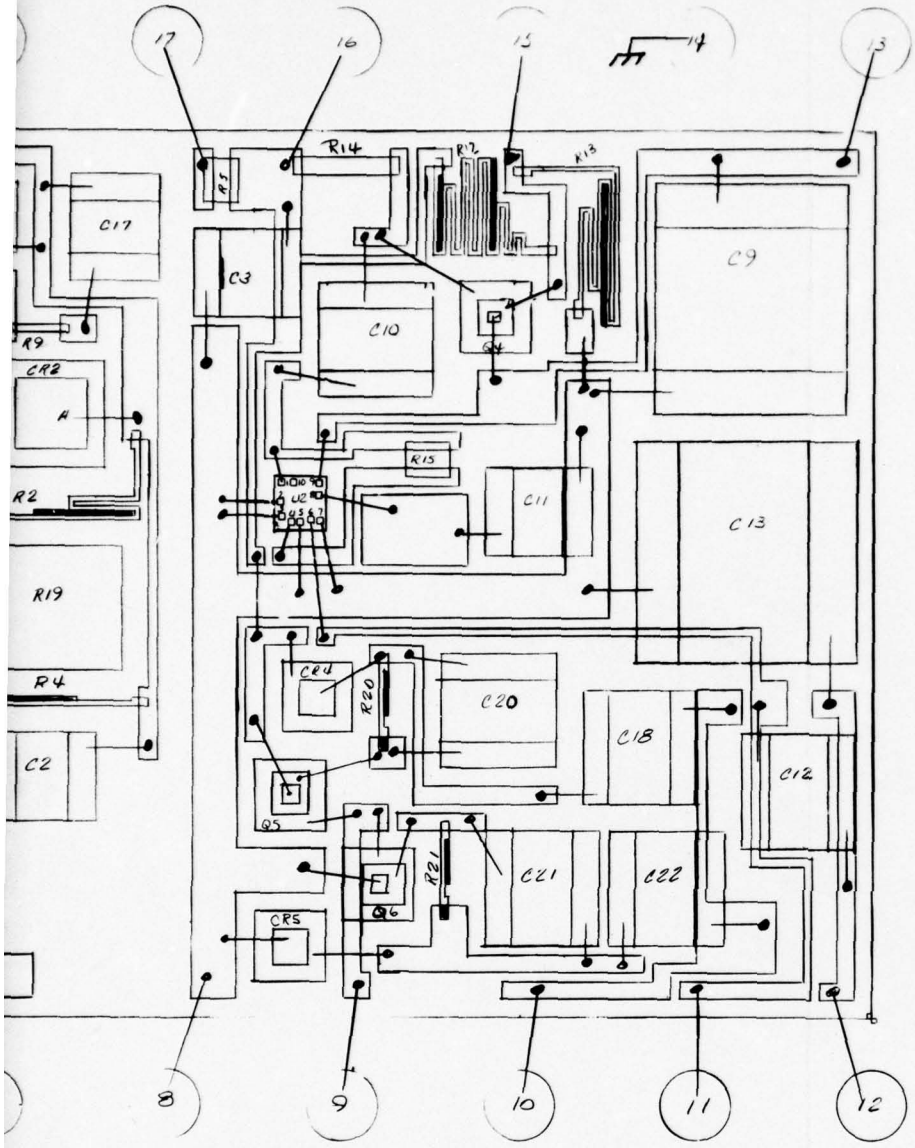


Figure 4-16. 24-Pin Metal Thin-Film Enclosure.



SYMBOL	TOL	MIN	NOM	MAX	COUNT
R1	1%	9.9000	10.000	10.1000	45.0
R2	1%	11.9790	12.100	12.2210	54.0
R3	1%	29.7990	30.100	30.4010	135.0
R4	1%	5.5638	5.620	5.6762	25.0
R5, R15	10%	0.0900	0.100	0.1100	0.4
R6, R7, R8	5%	30.0200	31.600	33.1800	142.0
R9	5%	0.9500	1.000	1.0500	5.0
R10	5%	6.4695	6.810	7.1505	30.0
R12	5%	24.7950	26.100	27.4050	117.0
R13	5%	20.4250	21.500	22.5750	96.0
R16, R17	10%	45.9900	51.100	56.2100	230.0
R11, R14	10%	0.9000	1.000	1.1000	5.0
R18	5%	1.9000	2.000	2.1000	10.0
R20, R21	5%	2.0900	2.200	2.3100	10.0



NOTES:

1. TOP LEVEL: 632-3875-001

2. SUBSTRATE SIZE

   X = 12.700 [.500] STEP 3
   Y = 27.940 [1.100] STEP 1

3. UNLESS OTHERWISE SPECIFIED ALL LINES DRAWN ON GRID ARE TO BE DEFINED AS BEING HALFWAY BETWEEN TWO GRID LINES.
4. ALL RESISTORS ARE 200 OHMS PER SQUARE.

PARTS LIST

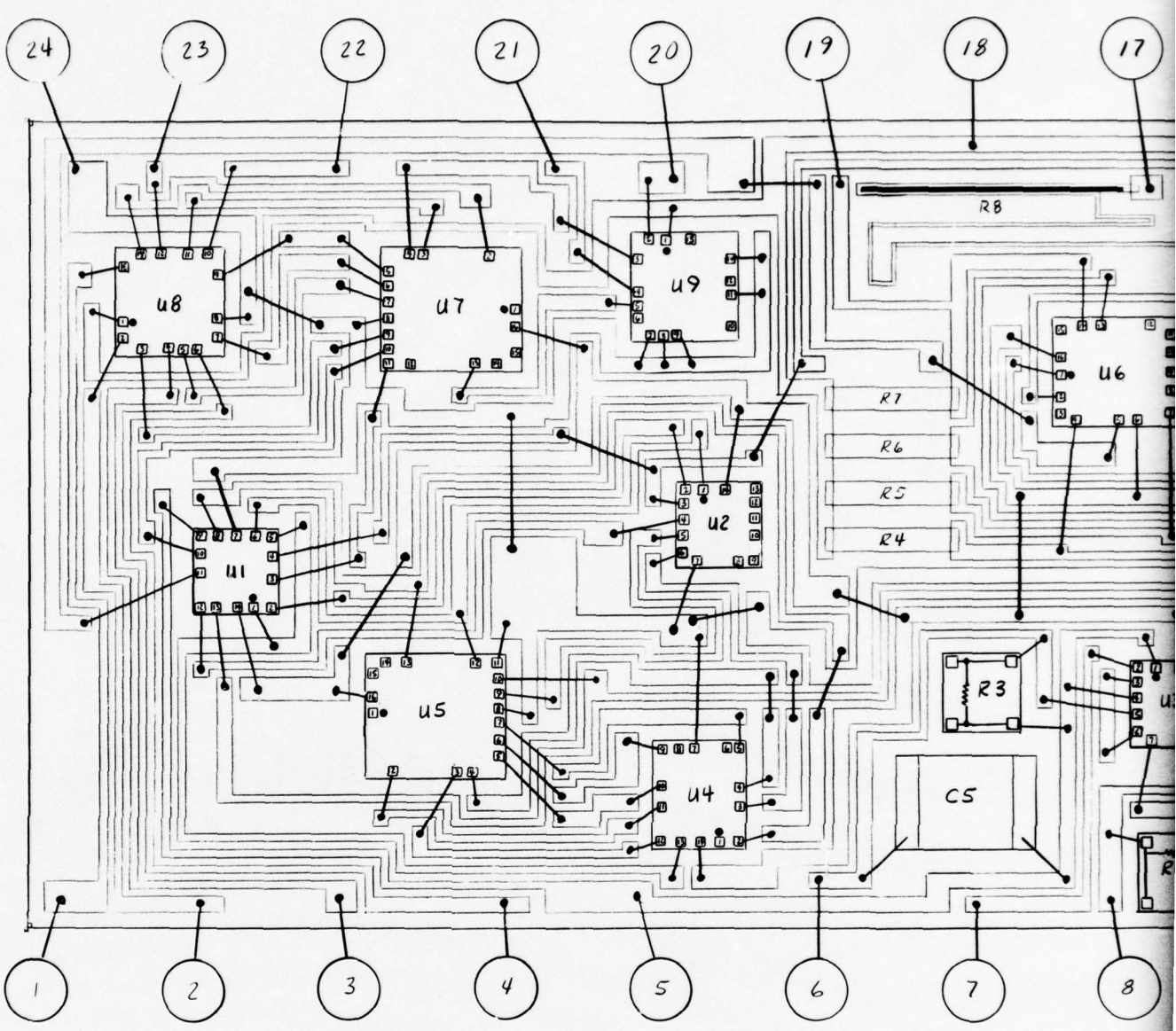
QTY	ITEM NO	PART OR IDENTIFYING NO	NAME	DESCRIPTION
2.0	37	351-9900-010	TAB	.060 X .060
8.0	36	351-9900-050	TAB	.040 X .040
0.0	35	669-8150-001	PTS	
0.0	34	636-1624-001	REF DWG	MK TOOL
0.0	33	636-1623-001	REF DWG	AW 3 SYMBOLS
0.0	32	636-1622-001	REF DWG	AW 2 RESISTOR
0.0	31	636-1621-001	REF DWG	AW 1 CONDUCTOR
0.0	30	636-1620-001	REF DWG	SCHEMATIC
1.0	29	190-0422-040	COVER	TEKFORM 20264
1.0	28		CASE	TEKFORM 20169
3.0	27	351-9941-140	PREFORM	.125 X .130
2.0	26	351-9941-540	PREFORM	.105 X .135
1.0	25	351-9941-630	PREFORM	.070 X .100
1.0	24	351-9941-100	PREFORM	.085 X .085
2.0	23	351-9941-460	PREFORM	.060 X .060
1.0	22	351-9941-260	PREFORM	.035 X .035
8.0	21	351-9941-450	PREFORM	.050 X .070
9.0	20	351-9941-280	PREFORM	.070 X .070
8.0	19	351-9941-240	PREFORM	.040 X .040
1.0	18	351-4037-040	CAP	.001 MF
1.0	17	351-4036-570	CAP	68 PF
3.0	16	351-4036-550	CAP	56 PF
3.0	15	351-4036-700	CAP	300 PF
2.0	14	351-4036-450	CAP	22 PF
2.0	13	351-4046-430	CAP	.1 MF
7.0	12	351-4046-310	CAP	.01 MF
1.0	11	351-9006-230	RES CHIP	1 MEG
1.0	10	351-3044-210	DIODE	IN4567A
1.0	9	351-3025-120	DIODE	IN754A
1.0	8	351-3025-090	DIODE	IN751A
1.0	7	351-6120-010	IC CHIP	MC1550
1.0	6	351-6121-010	IC CHIP	UA776
3.0	5	351-5070-010	TRANST	2N918
2.0	4	351-5003-010	TRANST	2N2907
2.0	3	351-3003-010	DIODE	IN4454
2.0	2	351-4036-540	CAP	51 PF
1.0	1	351-5005-010	TRANST	2N2222

Figure 4-17. U101-Oscillator/Amplifier, Thin-Film, Layout/Bo

PARTS LIST

EM D	PART OR IDENTIFYING NO	NAME	DESCRIPTION	UM	MN	USED ON
	351-9900-010	TAB	.060 X .060			23
	351-9900-050	TAB	.040 X .040			19
	669-8150-001	PTS				
	636-1624-001	REF DWG	MK TOOL			
	636-1623-001	REF DWG	AW 3 SYMBOLS			
2	636-1622-001	REF DWG	AW 2 RESISTOR			
1	636-1621-001	REF DWG	AW 1 CONDUCTOR			
0	636-1620-001	REF DWG	SCHEMATIC			
9	190-0422-040	COVER	TEKFORM 20264			
8		CASE	TEKFORM 20169			
7	351-9941-140	PREFORM	.125 X .130			
6	351-9941-540	PREFORM	.105 X .135			
5	351-9941-630	PREFORM	.070 X .100			
4	351-9941-100	PREFORM	.085 X .085			
3	351-9941-460	PREFORM	.060 X .060			
2	351-9941-260	PREFORM	.035 X .035			
1	351-9941-450	PREFORM	.050 X .070			
0	351-9941-280	PREFORM	.070 X .070			
19	351-9941-240	PREFORM	.040 X .040			
18	351-4037-040	CAP	.001 MF			20
17	351-4036-570	CAP	68 PF			20
16	351-4036-550	CAP	56 PF			20
15	351-4036-700	CAP	300 PF			27
14	351-4036-450	CAP	22 PF			20
13	351-4046-430	CAP	.1 MF			26
12	351-4046-310	CAP	.01 MF			21
11	351-9006-230	RES CHIP	1 MEG			25
10	351-3044-210	DIODE	IN4567A			24
9	351-3025-120	DIODE	IN754A			37
8	351-3025-090	DIODE	IN751A			37
7	351-6120-010	IC CHIP	MC1550			22
6	351-6121-010	IC CHIP	UA776			21
5	351-5070-010	TRANST	2N918			36
4	351-5003-010	TRANST	2N2907			36
3	351-3003-010	DIODE	IN4454			36
2	351-4036-540	CAP	51 PF			20
1	351-5005-010	TRANST	2N2222			36

lator/Amplifier, Thin-Film, Layout/Bonding Diagram.

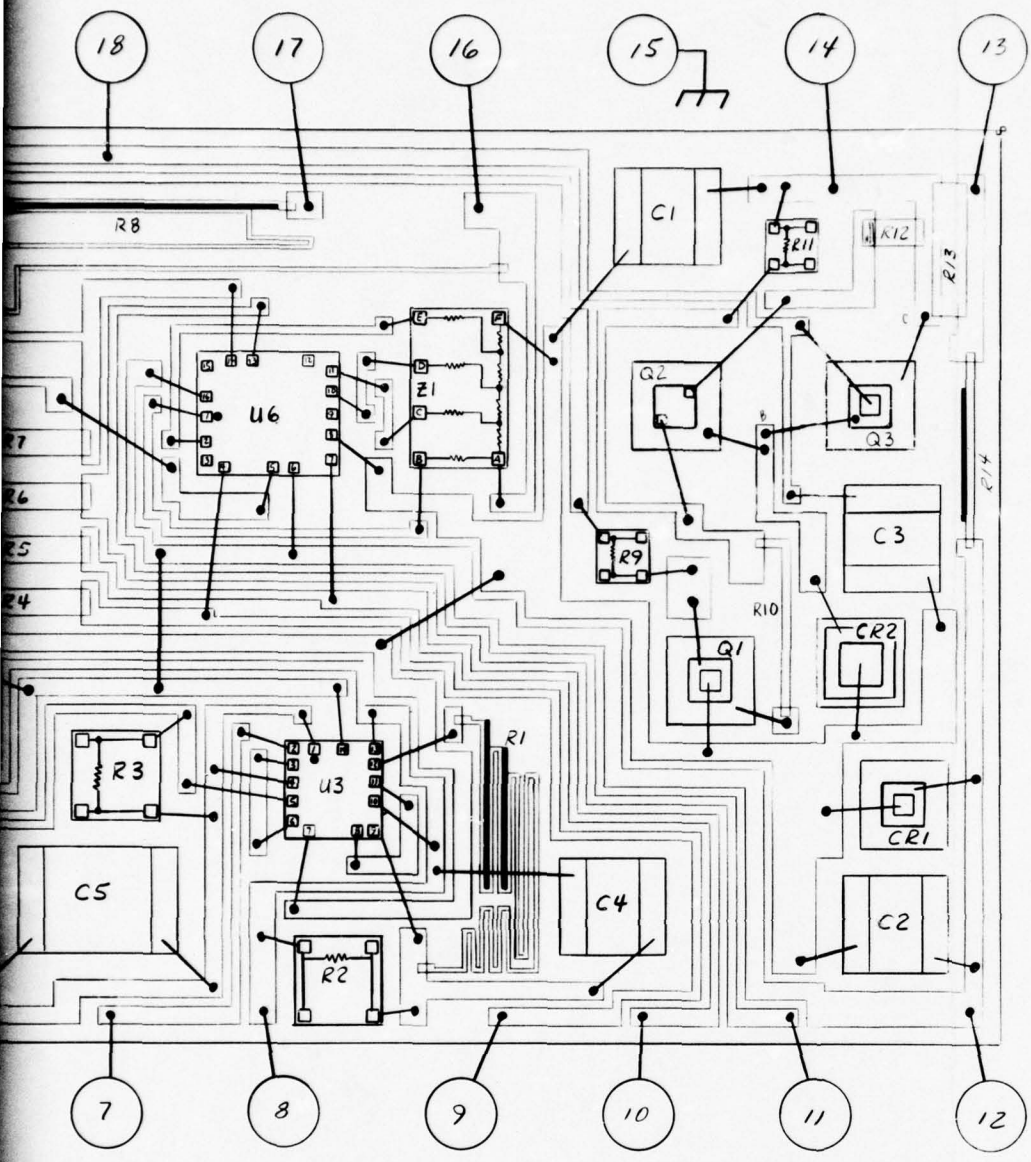


NOTES:
1. TOP LEVEL 632-3876-001

2. SUBSTRATE SIZE X = 28.194 [1.110] Y = 13.081 [0.515]
   STEP X = 1 Y = 3

3. UNLESS OTHERWISE SPECIFIED, ALL LINES NOT DRAWN ON GRID ARE TO BE DEFINED AS BEING HALFWAY BETWEEN TWO GRID LINES.
4. THE FOLLOWING RESISTORS ARE 200 OHMS PER SQUARE
   R1, R4, R5, R6, R7, R8, R10, R12, R13, R14

SYMBOL	TOL
R1, R8	±1%
R4, 5, 6, 7	±5%
R10	±5%
R12	±5%
R13	±5%
R14	±1%



SYMBOL	TOL	MIN	NOM	MAX	SQUARE COUNT
R1, R8	±1%	5.38K	51.9K	52.4K	233.0
R4, 5, 6, 7	±5%	.950K	1.0K	1.010K	5.0
R10	±5%	3.70K	3.9K	4.095K	20.0
R12	±5%	.313K	.330K	.346K	1.5
R13	±5%	.031K	.033K	.0347K	0.1333
R14	±1%	3.455K	3.49K	3.525K	0

PARTS LIST

QTY	ITEM NO	PART OR IDENTIFYING NO	NAME	DESCRIPTIO
REF	37	636-1643-001	SCHEMATIC	
REF	36	636-1644-001	ARTWORK	CONDUCTOR
REF	35	636-1645-001	ARTWORK	RESISTOR
REF	34	636-1646-001	ARTWORK	MARKING TO
2.0	33	351-9941-530	PREFORM	50 X 90
1.0	32	351-9941-450	PREFORM	50 X 70
3.0	31	351-9941-280	PREFORM	70 X 70
5.0	30	351-9941-270	PREFORM	50 X 50
2.0	29	351-9941-260	PREFORM	35 X 35
1.0	28	351-9941-240	PREFORM	40 X 40
2.0	27	351-9941-100	PREFORM	85 X 85
7.0	26	351-9941-010	PREFORM	50 X 55
1.0	25	351-5005-010	TRANSISTOR	2N2222
1.0	24		PREFORM	SEALING
1.0	23	190-0422-040	COVER	
1.0	22		CASE	
	21		EPOXY	CONDUCTIV
1.0	20	351-9923-070	TAB	MOLY 50 X 5
3.0	19	351-9900-060	TAB	KOVAR 50 X
1.0	18	351-9900-050	TAB	KOVAR 40 X
1.0	17	351-9032-150	RESISTOR	CHIP 39K
1.0	16	351-9032-170	RESISTOR	CHIP 47K
2.0	15	351-9032-410	RESISTOR	CHIP 470K
1.0	14	351-3059-050	DIODE	MZC4625
1.0	13	351-3025-100	DIODE	IN752A
3.0	12	351-4046-310	CAPACITOR	0.01 MF ±10
1.0	11	351-4041-270	CAPACITOR	510PENP0 ±
1.0	10	351-4041-200	CAPACITOR	330 PFNPO
1.0	9	351-5003-010	TRANSISTOR	2N2907
1.0	8	351-5005-010	TRANSISTOR	2N2222
1.0	7	351-9042-550	RESISTOR	ARRAY
2.0	6		1C	CD4069
1.0	5		1C	CD4068
2.0	4		1C	CD4050
1.0	3	351-6642-110	1C	CD4042
2.0	2		1C	CD4040
1.0	1	351-6642-020	1C	CD4001

Figure 4-18. U201-Digital Network, Thin-Film, Layout/

PARTS LIST

PART OR IDENTIFYING NO	NAME	DESCRIPTION	UM	MN	ALTN PREF	USED ON
636-1643-001	SCHEMATIC					
636-1644-001	ARTWORK	CONDUCTOR				
636-1645-001	ARTWORK	RESISTOR				
636-1646-001	ARTWORK	MARKING TOOL				
351-9941-530	PREFORM	50 X 90				
351-9941-450	PREFORM	50 X 70				
351-9941-280	PREFORM	70 X 70				
351-9941-270	PREFORM	50 X 50				
351-9941-260	PREFORM	35 X 35				
351-9941-240	PREFORM	40 X 40				
351-9941-100	PREFORM	85 X 85				
351-9941-010	PREFORM	50 X 55				
351-5005-010	TRANSISTOR	2N2222				20
	PREFORM	SEALING				
190-0422-040	COVER					
	CASE					
	EPOXY	CONDUCTIVE				
351-9923-070	TAB	MOLY 50 X 50				21
351-9900-060	TAB	KOVAR 50 X 50				30
351-9900-050	TAB	KOVAR 40 X 40				28
351-9032-150	RESISTOR	CHIP 39K				29
351-9032-170	RESISTOR	CHIP 47K				29
351-9032-410	RESISTOR	CHIP 470K				30
351-3059-050	DIODE	MZC4625				19
351-3025-100	DIODE	IN752A				19
351-4046-310	CAPACITOR	0.01 MF ±10%				26
351-4041-270	CAPACITOR	510PENP0 ±5%				33
351-4041-200	CAPACITOR	330 PFNPO ±5%				26
351-5003-010	TRANSISTOR	2N2907				18
351-5005-010	TRANSISTOR	2N2222				19
351-9042-550	RESISTOR	ARRAY				33
	1C	CD4069				26
	1C	CD4068				32
	1C	CD4050				31
351-6642-110	1C	CD4042				31
	1C	CD4040				27
351-6642-020	1C	CD4001				26

tal Network, Thin-Film, Layout/Bonding Diagram.

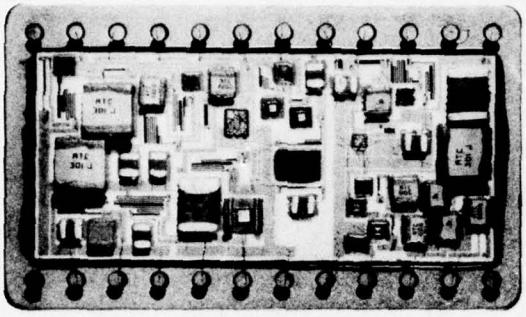


Figure 4-19. Coarse Oscillator Package, Hybrid Circuitry.

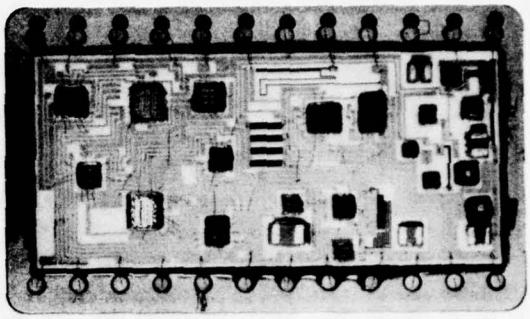


Figure 4-20. Digital Package, Hybrid Circuitry.

Thermal transient behavior and warmup performance have been studied and improved by testing several variations of this basic configuration, such as copper foil wrap on the glass crystal. For instance, thermal transient performance could be improved if the fine compensation thermistor, RT201, is mounted on the crystal, but spectral purity would have been degraded since RT201 is in a 50- to 100-kHz RC oscillator loop.

4.7 CRYSTALS

The success of building 5 pp 10^8 tcxo's greatly depends on the success of obtaining crystals that exhibit smooth frequency-temperature (F-T) characteristics, small F-T retrace errors, and low aging. Based on experience as well as published performance levels obtained on USAEC contracts DA28-043-AMC-02183 (E)[9] and DA28-043-AMC-01325(E), [10] specifications for high quality tcxo cyrstals were drawn; a summary appears in table 4-3. Crystals were ordered from the performers of the above two USAEC contracts, then tested; tests were performed on available crystals from other sources as well.

4.7.1 F-T Characteristics

For a seemingly routine parameter, frequency deviation between turning points proved to be troublesome to some crystal manufacturers. Crystals with deviation up to 50 ppm were accepted from one vendor. These proved to be compensatable as this put the upper turning point near +80 °C and saved use of additional thermistor/resistor network parts usually required when operating much above the crystal turning point.

F-T characteristics such as those in figure 4-26 were recorded on all crystals, using the test setup shown in figure 4-27. The Collins vector voltmeter crystal test set has been described previously.[11] Frequency and resistance characteristics were recorded continuously as temperature increased linearly at 1 °C per minute.

4.7.2 Retrace of F-T Characteristics

Previous experience at Collins showed that, at least for a few crystals, the amount of retrace error was dependent on the highest temperature to which the crystal had been recently exposed. Recordings in figure 4-28 demonstrate this phenomenon in a tcxo;

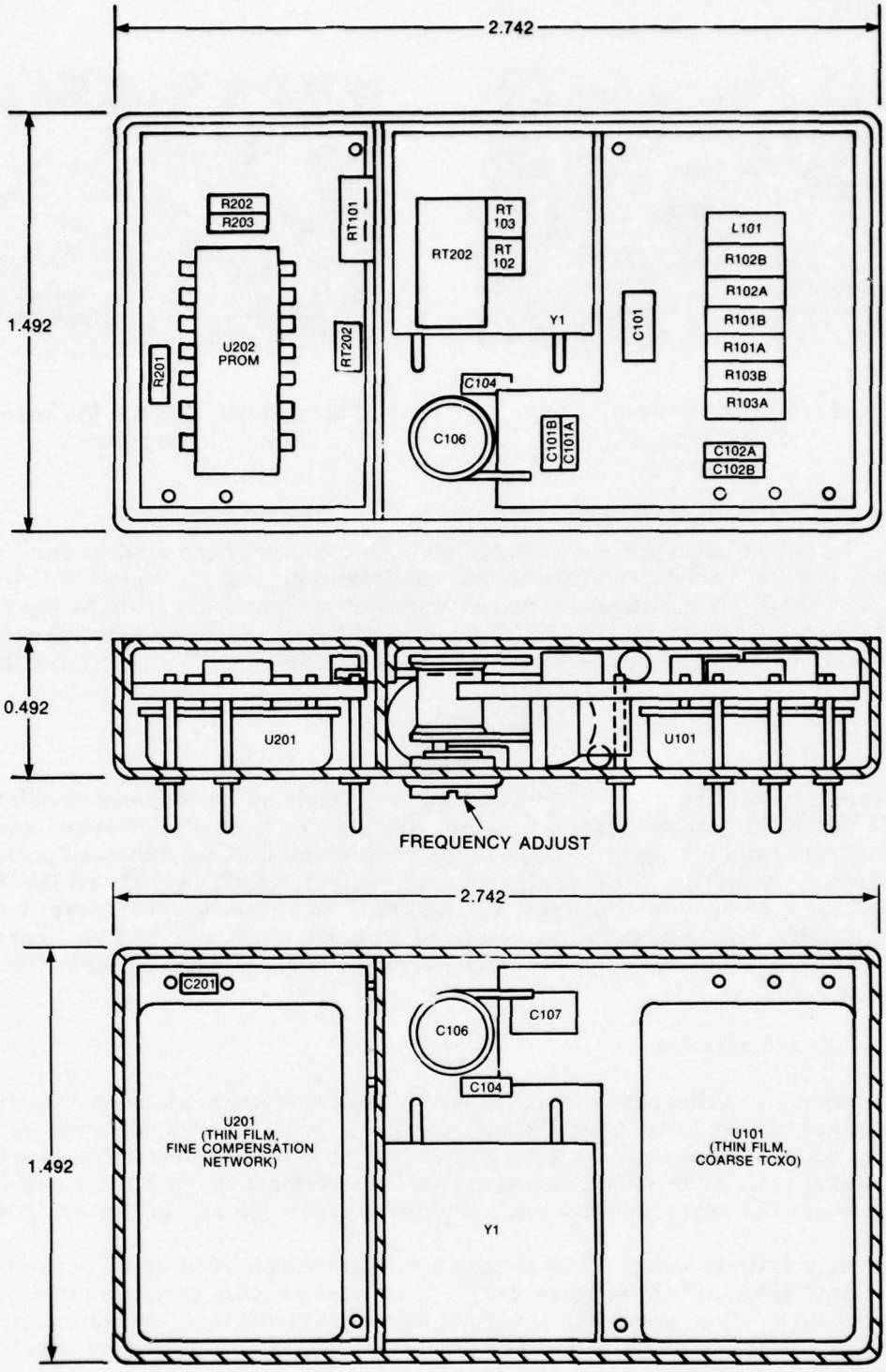


Figure 4-21. 2-Cubic-Inch TCXO Packaging Concept.

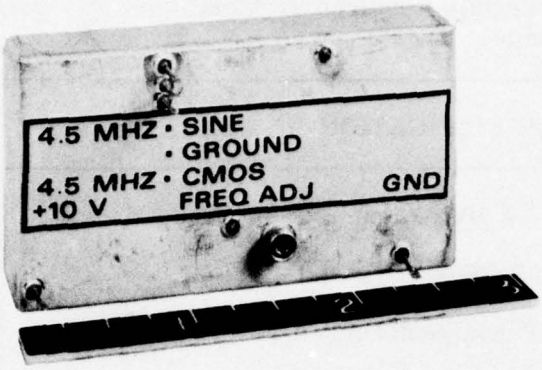


Figure 4-22. HSTCXO, Bottom View.

Figure 4-23. HSTCXO, Top View.

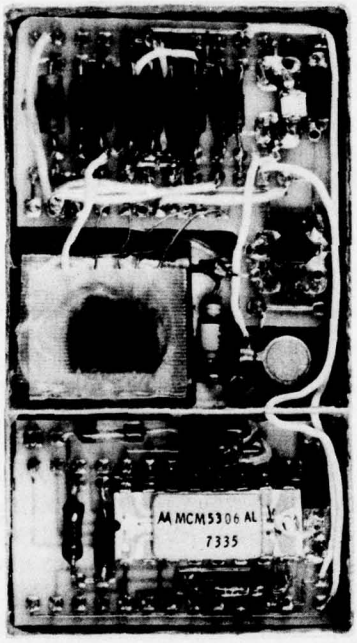


Figure 4-24. HSTCXO, Lids Removed, Top View.

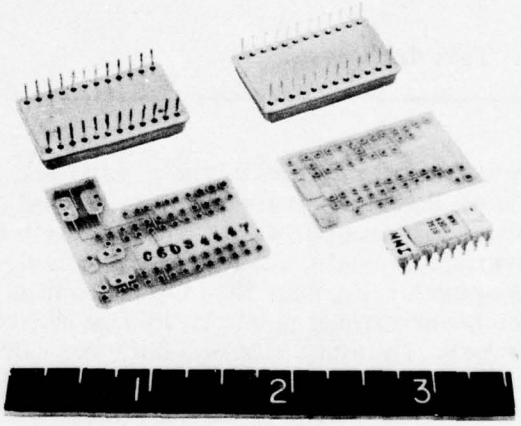


Figure 4-25. Hybrid Packages and PC Boards, Bottom View.

Table 4-3. Specifications for Crystals Required To Meet HSTCXO Requirements.

PARAMETER	SPECIFICATION
Frequency	4.5 MHz ±5 ppm at +30 °C
Load	32 pF
Type	Fundamental AT-cut
Holder	Coldweld HC-6/U, Glass HC-27/U
Resistance	10-Ω max, -46 to +85 °C
TC	45 ±5 ppm between turning points
Pullability	160 ±20 ppm, series to 32 pF
Aging	5 pp 10^{10}/day after 2 weeks storage at the upper turning point (UTP)
Frequency-temperature retrace error	3 pp 10^{8} max, measured at the lower turning point (LTP) after exposure to +25 °C for 16 hr and after exposure to +100 °C for 1 hr
Test drive level	10 μW into 10 Ω

subsequent tests proved the crystal had the same characteristics. Figure 4-28 also shows that the retrace error is largest (about 7 pp 10^{7}) at -55 °C and diminishes to near zero around +45 °C. Admittedly this example may not be representative of even average crystals, but it appears to indicate retrace data should be measured at low temperatures rather than high. To minimize errors due to temperature instability, the lower turning point (LTP) was chosen as the temperature for measuring retrace errors. Dynamic data was obtained using two test systems. One was the setup shown in figure 4-27, and the other was identical except that the vector voltmeter (VVM) test set was replaced by a Pierce oscillator. The profile of temperature excursions is shown in figure 4-29. The reference run is taken after any desired preconditioning of the test crystal, and then runs 2 and 3 are compared to the reference. Note that if retrace data were retraceable, runs 2 and 3 should give identical results. A comparison of data is shown in table 4-4.

In general, the results agree; but the oscillator data repeated better, usually within 4 pp 10^{9} at the LTP for identical temperature runs and thermal histories. Most crystals appear to exhibit retrace errors of 1 to 3 pp 10^{7} at the LTP (agreeing well with figure 4-28), although two crystals (A-107 and D-1) retraced within 3 pp 10^{8} without reason.

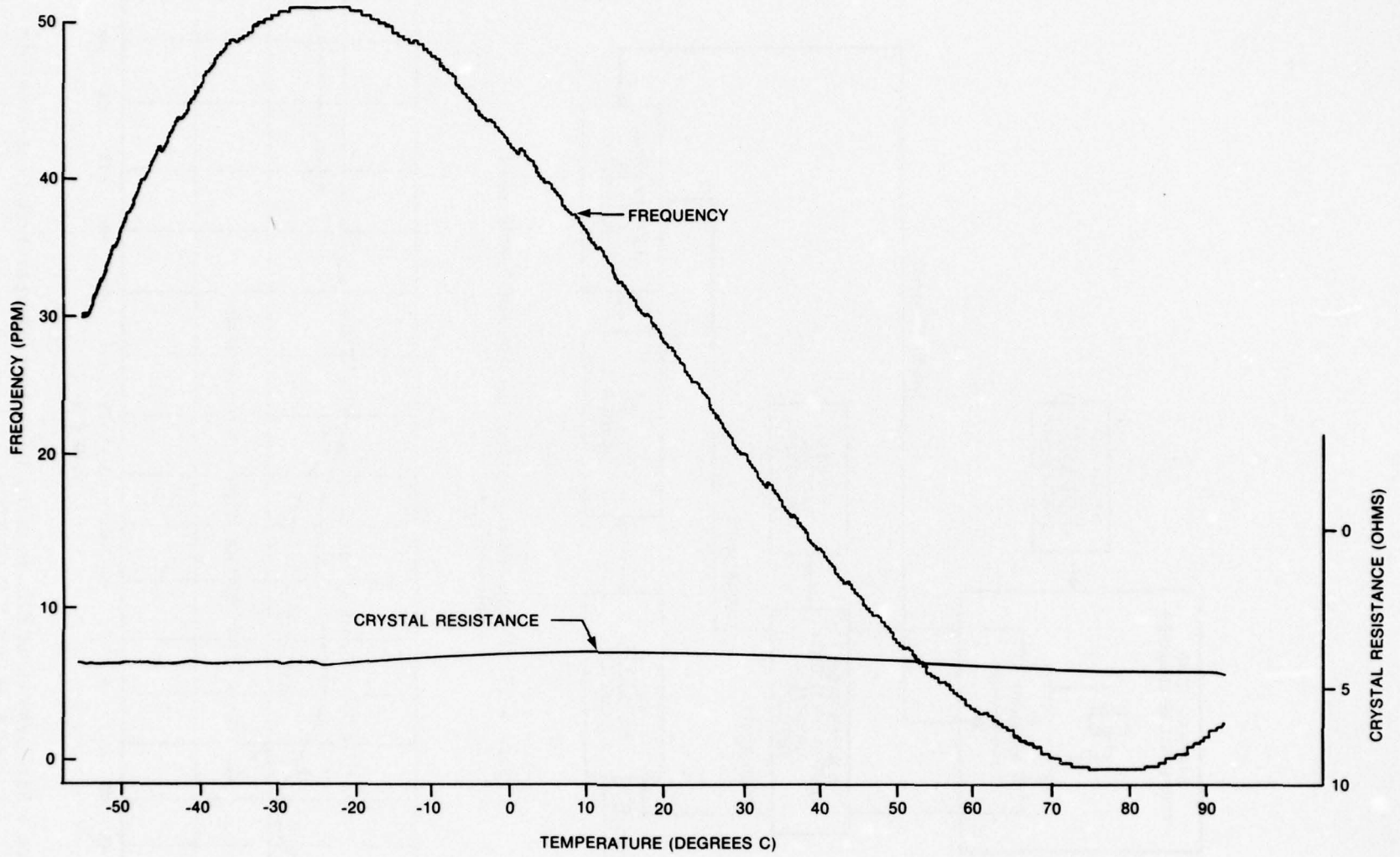


Figure 4-26. Frequency and Resistance Vs Temperature Characteristics for a 4.5-MHz Crystal.

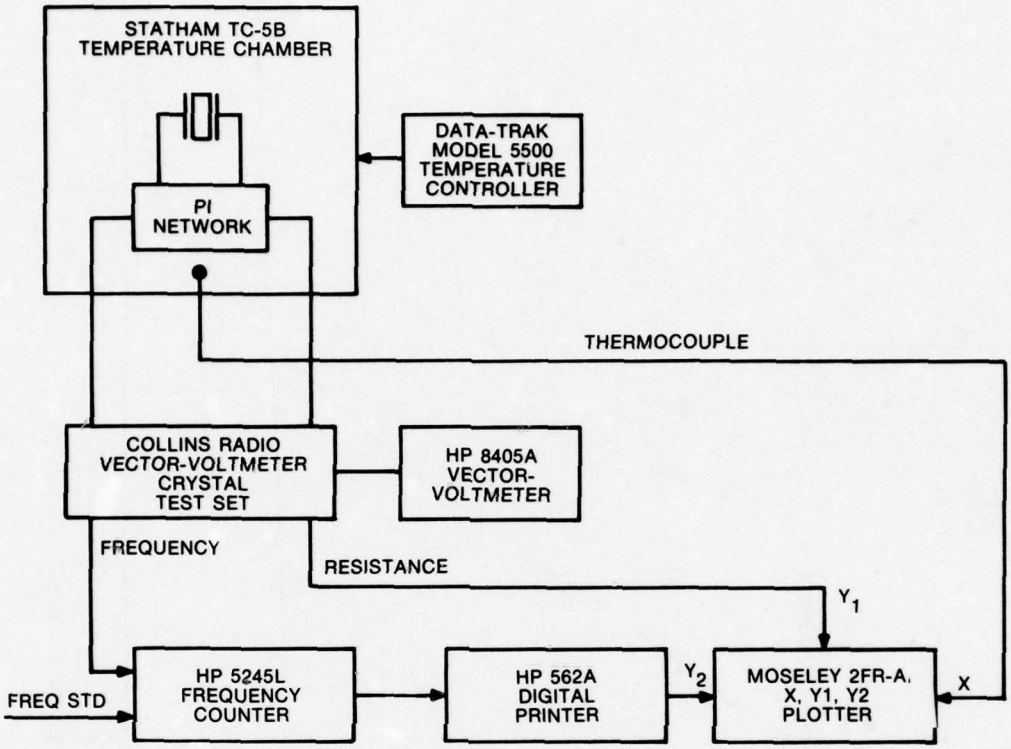


Figure 4-27. Measurement System for Crystal Hysteresis, Block Diagram.

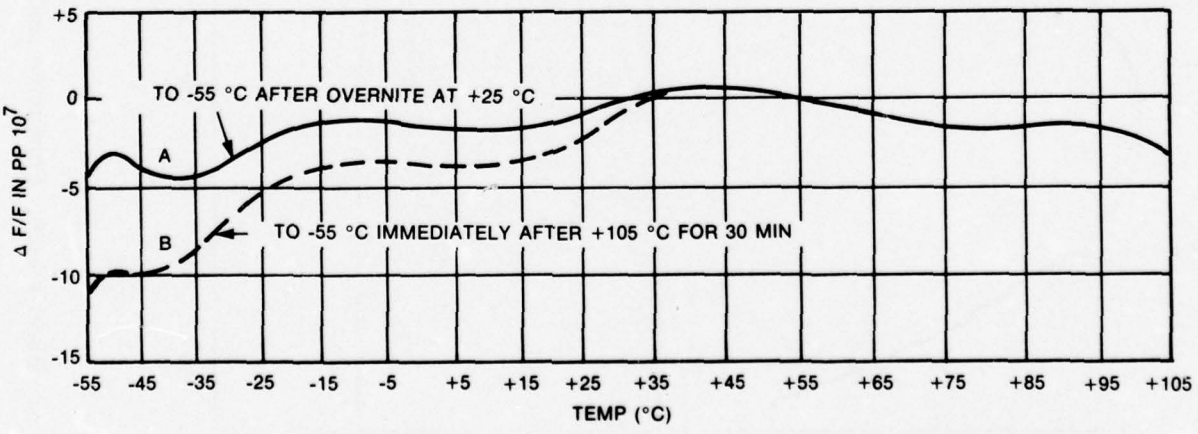


Figure 4-28. Hysteresis Effects in the Frequency-Temperature Characteristic of 4-MHz TCXO (SN8/52).

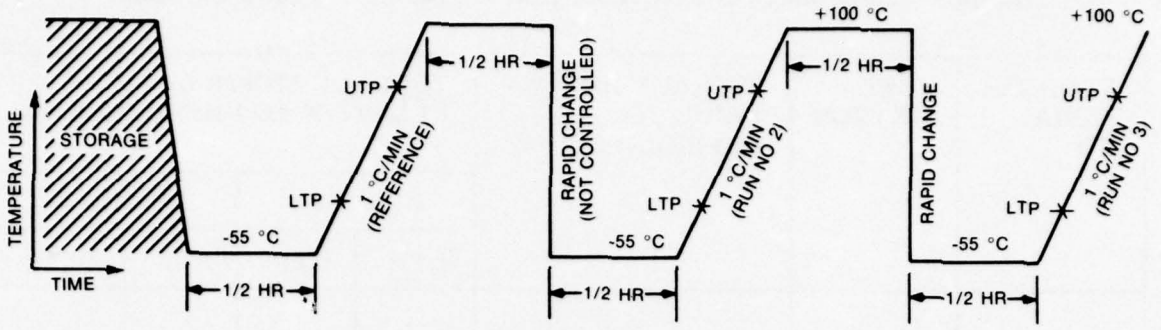


Figure 4-29. Temperature/Time Schedule for Oven Controller Used for Testing Crystal Hysteresis.

Reasons for the lack of data repeatability with the VVM crystal test set were not fully explored, although it was noted the crystal socket was worn and the connecting cables to the VVM were standard RG-142/U coaxial cables, possibly subject to movement from one temperature run to another. Possible improvements would be to solder the test crystal into the pi-network and to use coaxial cables with outer conductors made of solid copper. The VVM test set has previously exhibited a resettability accuracy of better than 2 pp 10^8, so frequency drift with no resetting should be even less if equipment is thoroughly warmed up.

Additional data obtained with crystal A-108 indicates that retrace error at the LTP is a function of storage time at room temperature. Starting with a run 2 as reference, additional runs were made, each with increasingly longer storage periods at room temperature after exposure to +100 °C. A sketch of the temperature/time schedule is shown in figure 4-30, and retrace data is plotted in figure 4-31. Note there is little scatter of data points around the average curve, especially for the first 20 hours of data.

It is interesting to note that this curve looks very much like the relaxation curve of a mechanical system having a time constant of about 4 hours. It follows, then, that 98 percent of the retrace error would be observed after four time constants, or 16 hours. Fortunately, most retrace data has been based on overnight storage, or about 15 to 16 hours.

An interesting speculation is that different relaxation curves would be obtained by storage at fixed temperatures other than room temperature. For temperatures higher than room ambient, the time constant must be increasingly shorter and the peak error less, since hysteresis curves merge as temperatures approach +100 °C. In fact, exposure of a crystal to +100 °C for only a short period seems to completely relax the crystal. Conversely, storage at low temperatures would probably exhibit very long time constants and even larger retrace errors. Since crystal retrace plays such an important part in the success or failure of this project, investigations were made into published papers that might give some insight into this problem. Very little information was found to be available in published form, so personal contact with crystal vendors was undertaken. It soon became obvious that an optimum mounting orientation could be found for minimum retrace, but this was not optimum for shock and vibration. From the received crystals purchased for this project, retrace measured at the lower

Table 4-4. Summary of Frequency Retrace Data for 5-MHz Crystals.

VENDOR-SERIAL NO	TEST METHOD	STORAGE HISTORY PRIOR TO REFERENCE RUN	RETRACE ERROR IN PP 10^8, RELATIVE TO REFERENCE RUN			
			RUN NO 2		RUN NO 3	
			LTP	UTP	LTP	UTP
A-107 (note 1)	VVM	46 h at RT	-2.0	-5.6	+2.6	+1.0
	OSC	24 h at RT	-1.0	+1.0		
A-108	VVM	59 h at RT	-21.1	+12.3	-21.1	+4.3
	Note 2	264 h at RT	-22.3	+12.0	-13.7	+13.3
	OSC	15 h at RT	-21.0	-0.3		
A-109	VVM	370 h at RT	-19.3	-7.3		
A-110	VVM	35 h at RT	-12.7	-4.0	-25.3	-3.0
	OSC	16.5 h at RT	-23.7	+1.7	-23.3	+2.0
A-111	VVM	11 h at RT	-12.3	+13.3	-11.7	+16.0
	OSC	15 h at RT	-13.7	+0.7	-13.7	+1.0
A-112	VVM	390 h at RT	-15.3	+4.0		
A-113	VVM	415 h at RT	-29.7	+1.3	-27.7	+5.0
B-1	VVM	>10 days at RT	-15.7	+4.7	-15.3	+4.3
C-1	VVM	>48 h at RT	-22.0	-19.6		
C-2	VVM	>48 h at RT	-30.3	-3.7	-27.0	-8.0
D-1	VVM	48 h at RT	-0.7		-3.7	
D-2	VVM	45 h at RT	-9.7	-5.3	-13.3	+1.7
D-3	VVM	69 h at RT	-8.3	-5.3	-9.0	0.0
D-4	VVM	93 h at RT	-20.3	+1.3		

NOTES:

1. Crystal A-107 was unit on loan from USAEC. Others were ordered for HSTCXO project.
2. Second VVM run on A-108 was attempt to reduce humidity effects by pressurizing temperature chamber with nitrogen gas.
3. Crystal drive in VVM was set at 10 μW into 10 Ω. Drive level in Pierce oscillator was similar.
4. Room temperature (RT) usually is 25 to 30 °C.

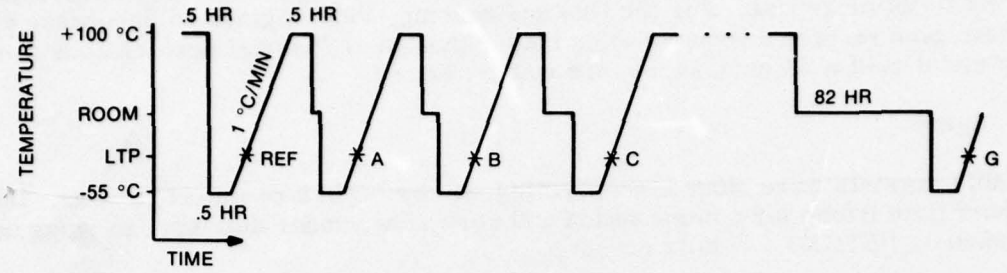


Figure 4-30. Profile of Temperature/Time Exposure for Crystal A-108.

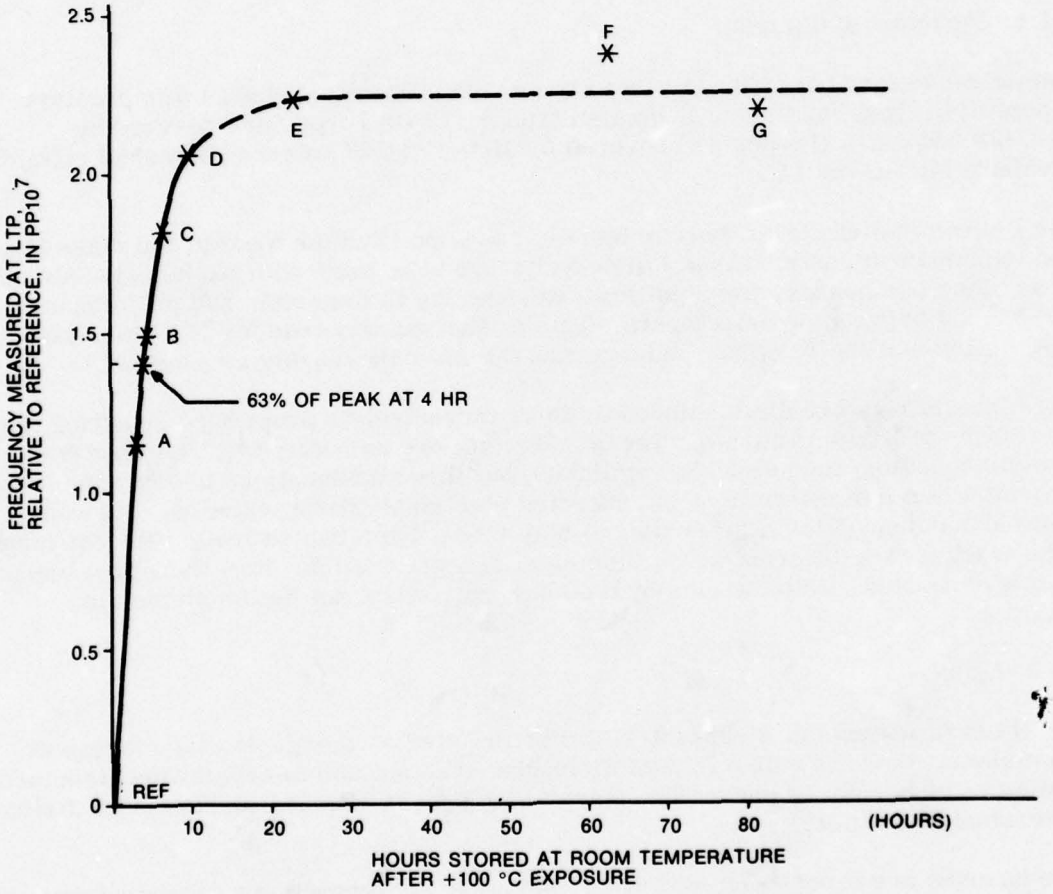


Figure 4-31. Plotted Retrace Data for Crystal A-108 as a Function of Storage Time at Room Temperature.

turning point was found to vary from 3 ppm to less than 1 pp 10^{-9} with no correlation from lot to lot or vendor. For the five engineering models, glass holders were chosen for their good retrace characteristics rather than their thermal performance which, in the metal cold weld enclosures, are usually better.

4.7.3 Aging

Available crystals were stored, unoperating, at +90 °C in a commercial oven. Due to the short time frame for compensation and very slow vendor delivery, no aging data was taken on HSTCXO 4.5-MHz crystals.

4.7.4 Capacitors

The possibility of capacitors causing frequency-temperature retrace errors was raised in the final report of the previous contract.[7] The following excerpts are quoted from a ceramic capacitor catalog.[12]

4.7.4.1 Capacitor Materials

Ceramic capacitors basically fall into two broad categories: class I (temperature-compensating types) and class II (high-K types). Class I types are covered by MIL-C-20 and class II types are covered by MIL-C-11015 or its established reliability equivalent, MIL-C-39014.

Class I ceramic dielectrics were originally based on titanium dioxide and class II are based on barium titanate. Class I dielectrics are also made with barium titanate as well as other compounds, and significant differences in materials and performance may be found between manufacturers. This is particularly true for NPO formulations which, because of their widespread use, are the most thoroughly researched.

Class II dielectrics are distinguished by their ferroelectric properties resulting from the influence of barium titanate. These materials are normally identified by their high dielectric constant, such as K1200 or K1800, but these designations are adequate only in providing a rough estimate of the expected electrical characteristics. A given dielectric constant (K1800, for instance) may result from two entirely different formulations, each with a different set of electrical characteristics. It is therefore important to specify class II dielectrics by the characteristics, not by the dielectric constant.

4.7.4.2 Aging

Class II ceramics exhibit a characteristic referred to as aging. During storage at room ambient, there is a decrease of dielectric constant due to crystalline structural adjustments of barium titanate. The magnitude of these changes increases as dielectric constant increases.

These changes are exponential with time, and aging is normally expressed as percent capacitance change per unit of time (such as two percent per decade). Time zero in such computations relates to the last exposure to a temperature in excess of 125 °C, and time is expressed hours. Figure 4-32 shows typical aging curves for characteristic B and C materials based on an aging rate of 2.5 percent for B and 4.0 percent for C. Characteristic A, being an NPO class I dielectric, has no aging.

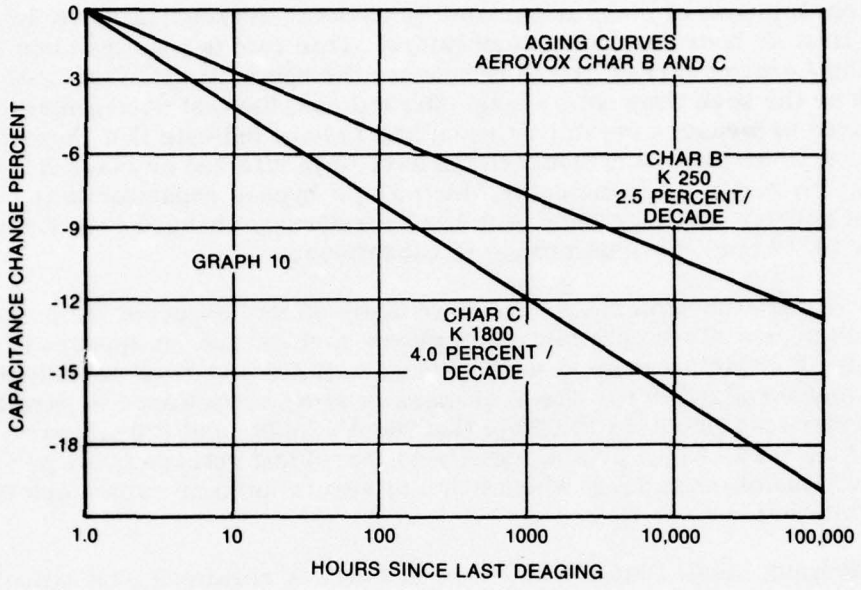


Figure 4-32. Graph 10 From Aerovox Product Specifier.

The aging process can be reversed by exposure to 125 °C and normally complete de-aging will occur at 150 °C. Both capacitance and dissipation factor will revert to the former 1.0-hour levels; then the aging process will resume.

Although the relationship may be a coincidence, such capacitance aging appears similar to the frequency-time relaxation curve of crystal A-108, which was tested on the previous contract. As shown in figures 4-30 and 4-31 (which are reproduced from the final report[7]), the majority of the frequency retrace error, or aging, took place in the first 10 to 15 hours. Since the oscillator used to test crystal A-108 contained a few class II bypass capacitors, it is worthwhile to consider capacitors for possible contributions to measured crystal retrace errors.

Note that de-aging of class II capacitors is said to be reversed by exposure to temperatures of 125 to 150 °C. To determine if de-aging also occurs at lower temperatures and to compare the retrace of capacitors for various class I capacitors, a number of capacitors were tested, using roughly the same temperature/time profile used to test crystals.

Various capacitors were measured with a General Radio 1673-A Automatic Capacitance Bridge and a Delta Design MK-2200 Temperature Chamber. Samples were

exposed to the temperature/time schedule sketched in figure 4-33. Data is summarized in figures 4-34, 4-35, and 4-36. Generally, each curve is the average of three samples of the same type. In each curve, the capacitance measured on the first exposure to +106 °C is used as reference.

The aging phenomenon of class II ceramic is obvious, decreasing about 1.5 percent during the first 20 hours at room temperature. This rate is less than half that predicted by the Aerovox curves, possibly because the upper temperature extreme was not as high or the soak time not as long. Regardless, the test does simulate the sequence used to measure crystal retrace, and results indicate that there is little chance that crystal retrace measurements have been affected by class II ceramic capacitors. To verify this conclusion, the 0.01-μF bypass capacitor in the oscillator used to test retrace was increased to 0.02 μF; frequency changed only 1.6×10^{-8}, or about 1.6×10^{-10} per 1 percent change in capacitance.

Figures 4-34 and 4-35 show the much lower aging effects expected from class I ceramics and other capacitors with low temperature coefficients. It appears the ATC 5.6- and 2.2-pF capacitors age about 1 percent over the 160-hour period; but possibly this is measurement error due to changes in stray capacitance in parallel with each unit under test (about 1 pF). Note that the ATC 470- and 620-pF parts are very stable. In fact, ATC[13] specifies aging effects (none) and retrace ($\leq$0.1 percent) for the ATC-100 line of capacitors, which helps to assure uniform capacitors for tuning crystal oscillators.

On the other hand, small DM5 micas, N030 monolythic ceramics, and silicon dioxide MOS capacitors also appear very stable with time and temperature; therefore, these parts are also suitable for tuning crystal oscillators, although retrace and aging are not closely controlled by specifications.

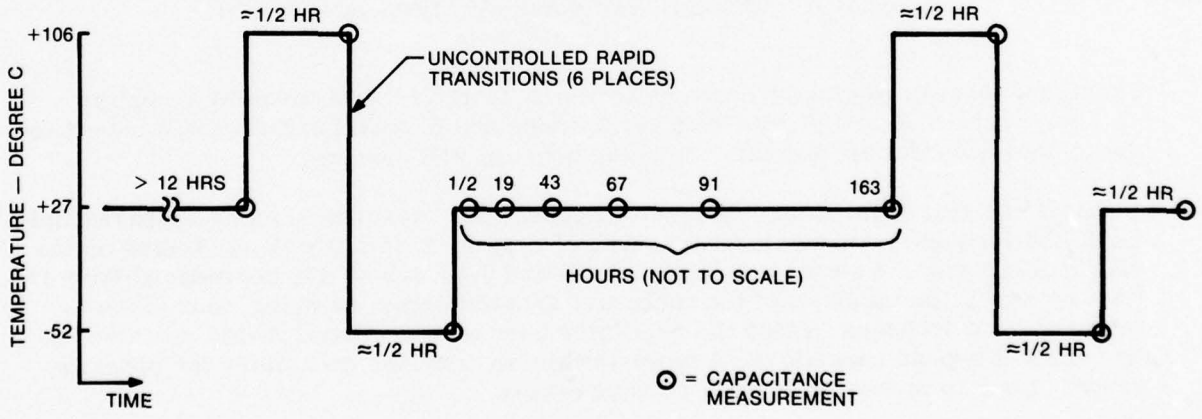


Figure 4-33. Temperature/Time Schedule for Oven Controller Used for Testing Stability of Capacitors.

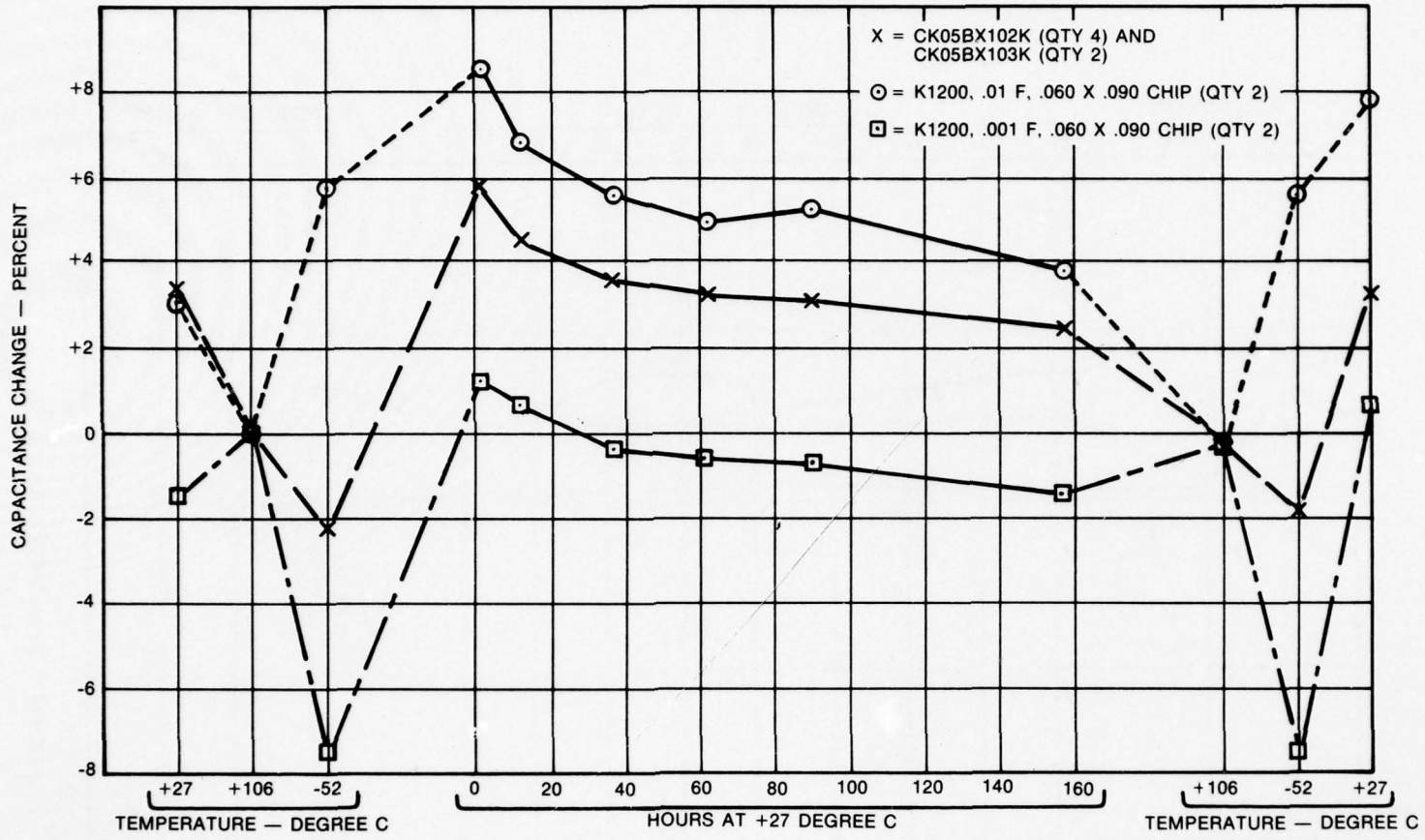


Figure 4-34. Time/Temperature Stability of Various High-K Ceramic Capacitors.

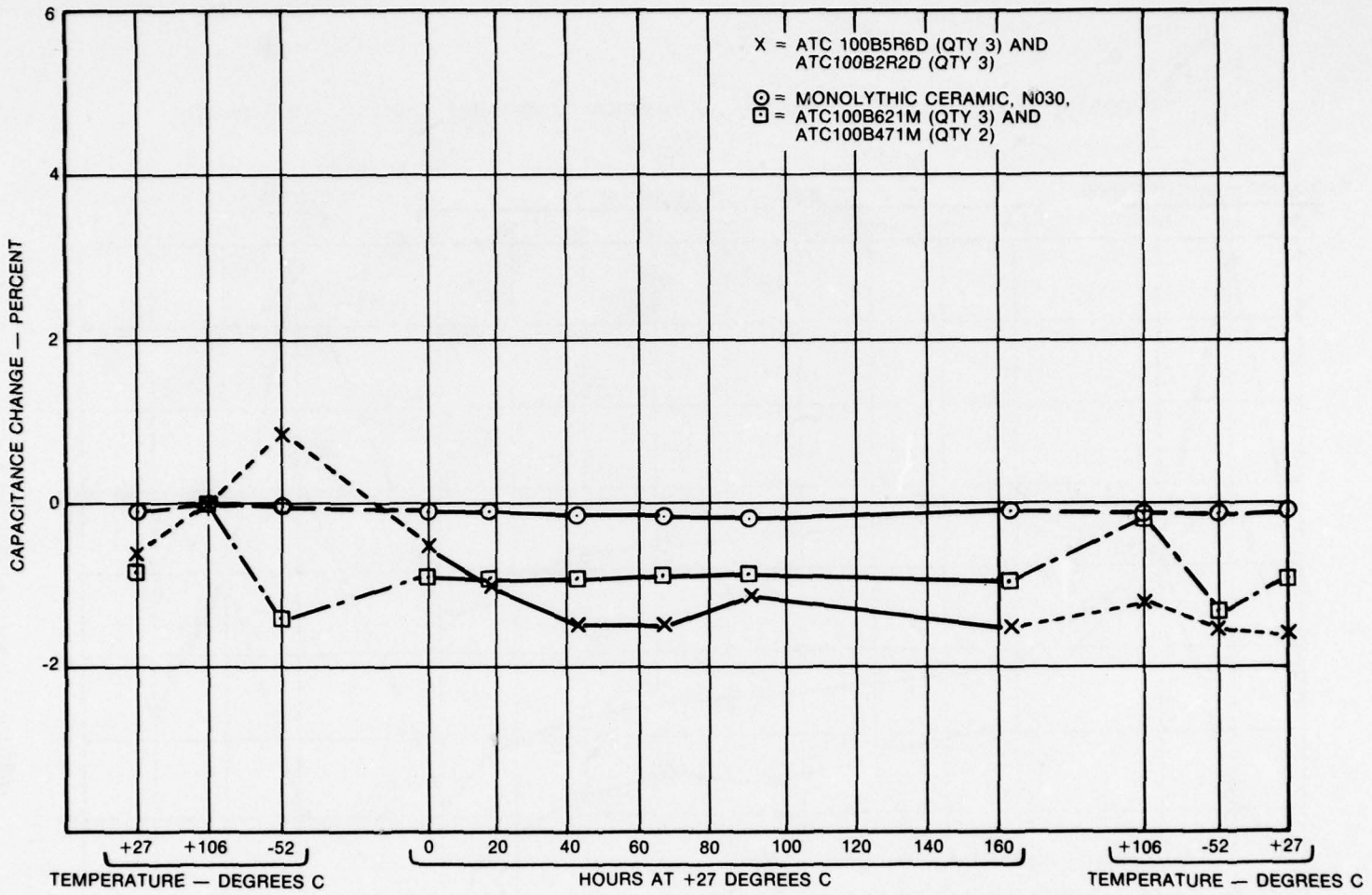


Figure 4-35. Time/Temperature Stability of Ceramic and Porcelain Low-TC Capacitors.

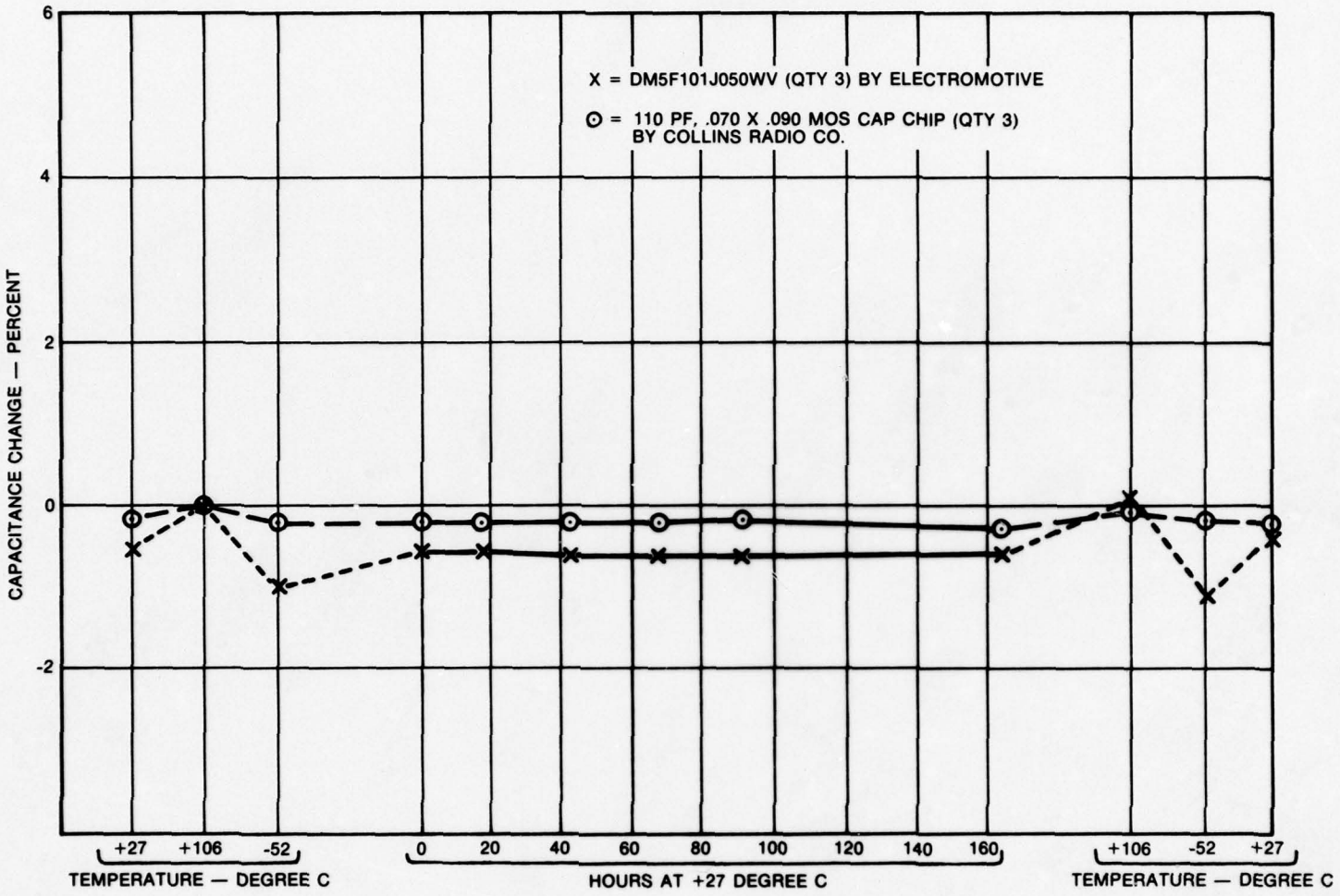


Figure 4-36. Time/Temperature Stability of Mica and Silicon Dioxide Capacitors.

Compensation to ±5 pp 10^8 requires a capability of accurately repeating test conditions. Instrumentation diagramed in figure 5-1 provides such capability if all equipments are maintained in proper working condition.

Stable and repeatable temperature settings are essential. As shown in figure 5-1, chamber temperature is monitored by a Fluke digital thermometer. Frequency stabilization at each set temperature is monitored with a frequency comparator and a multichannel recorder system capable of stepping through six oscillators every 2 minutes. Resolutions to 1 pp 10^9 can be obtained with 1-second counts. Using a stabilization criterion of 5 pp 10^9 maximum change in a 15-minute period, units under test are usually stable 45 minutes after a 5 °C temperature change.

In addition to instrumentation, the following compensation procedures were developed in the course of constructing ten HSTCXO models.

5.1 COARSE COMPENSATION

Connect the uncompensated unit to the interface adapter (figure 5-2), using a cabling harness (figure 5-3). Besides making power connections, this harness substitutes a big variable ROM (the HSTCXO test fixture/PROM programmer, figure 5-4) for the ROM to be installed in the digital compensation circuit. The interface adapter merely allows an operator to stop, hold, and read an address update by depressing a switch. Input pulses to the trigger latches are delayed by the monostable multivibrator (figure 5-5). Addresses are displayed on the test fixture in a decimal format using a 3-digit display. The test fixture also provides manual selection of ROM output words and displays the selected word in decimal format using a 2-digit display.

5.1.1 Initial Setup

Connect decade boxes or variable resistors as substitutes for R101, R102, and R103. (Refer to figures 4-8 and 4-12 for components selected by test.) Apply power to the test unit and install select components: C102 to set unit on frequency; C101 to set varactor sensitivity; R201 to set fine compensator step size (about 4 to 5 pp 10^8 for each of 16 steps); and R202 to set the change in ROM addresses with temperature (less than 256 states from -46 to +85 °C). Some of these selects are only estimated initially, then changed if so determined by temperature runs.

5.1.2 Temperature Runs

Precondition the tcxo components with at least three temperature cycles, each consisting of exposure to -46 °C and +85 °C for one hour. Then stabilize unit at room temperature for at least 10 hours.

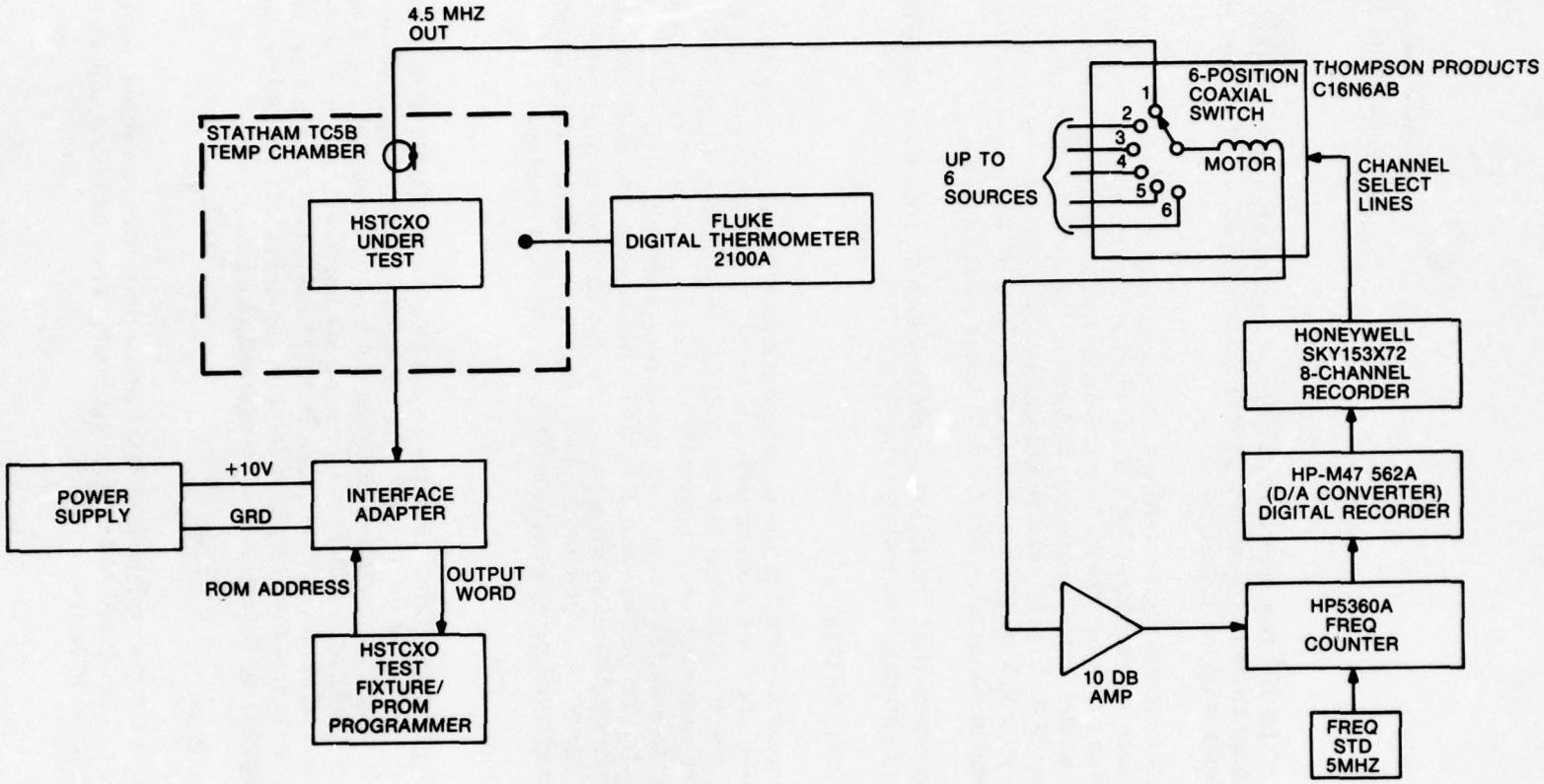


Figure 5-1. Instrumentation Diagram for Testing HSTCXO's.

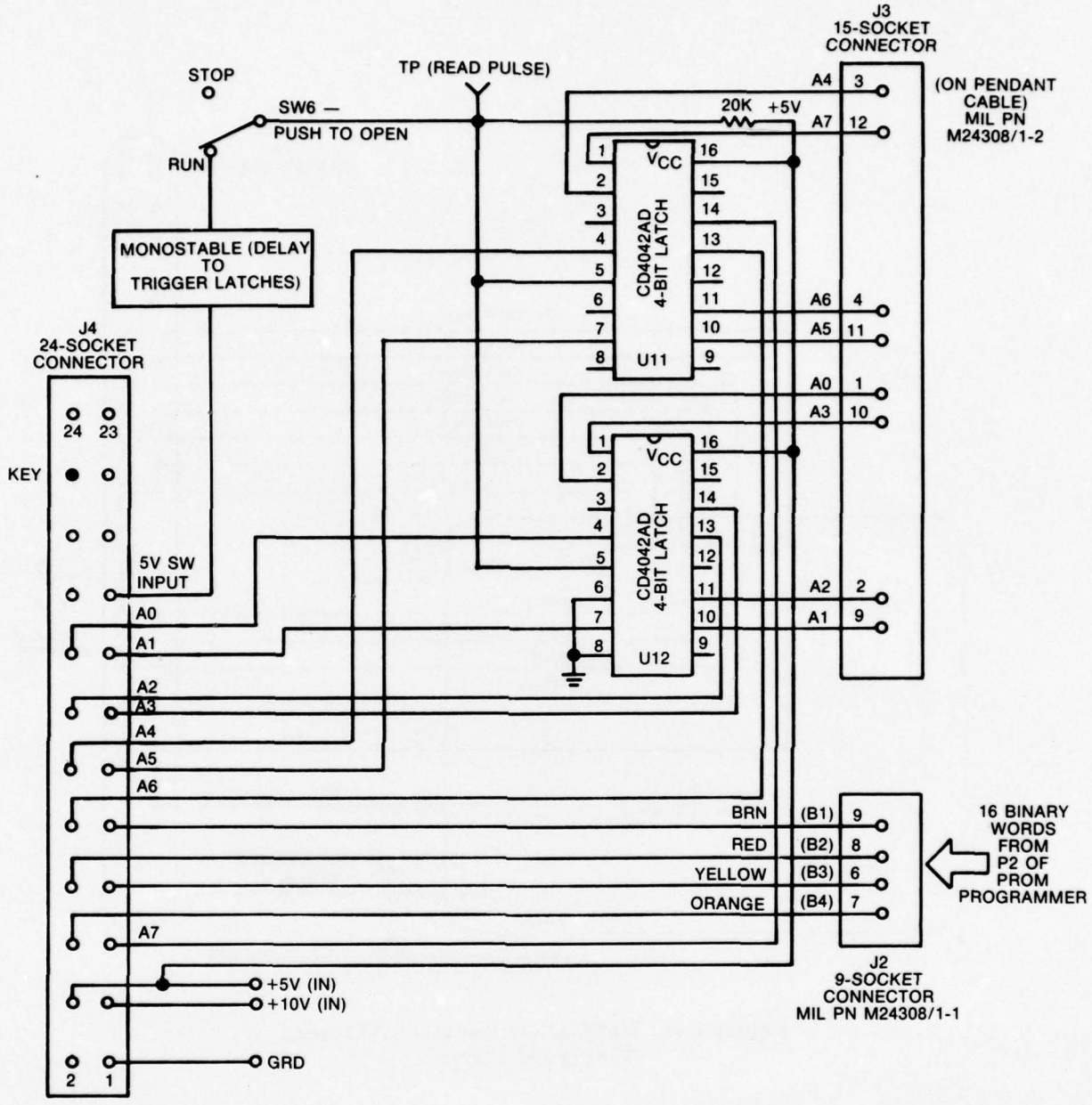


Figure 5-2. Interface Adapter From HSTCXO to Test Fixture/PROM Programmer, Wiring Diagram.

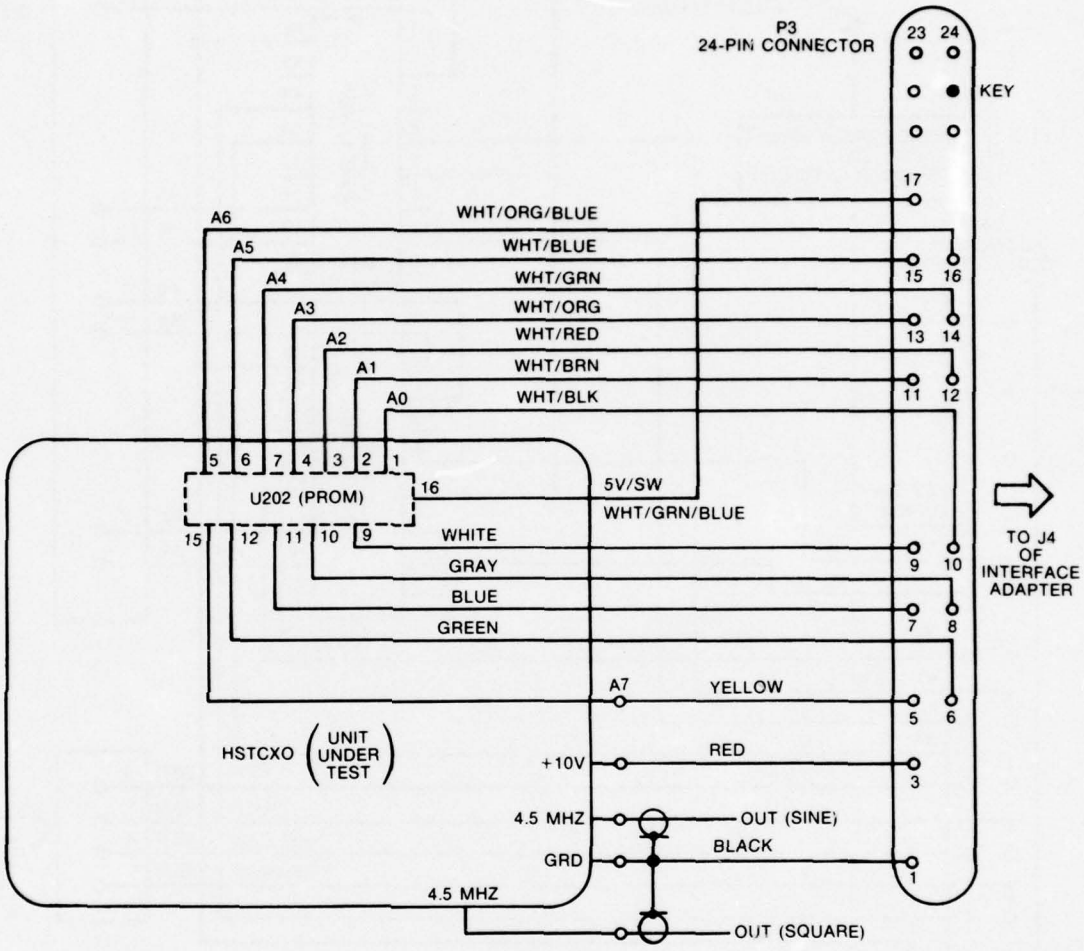
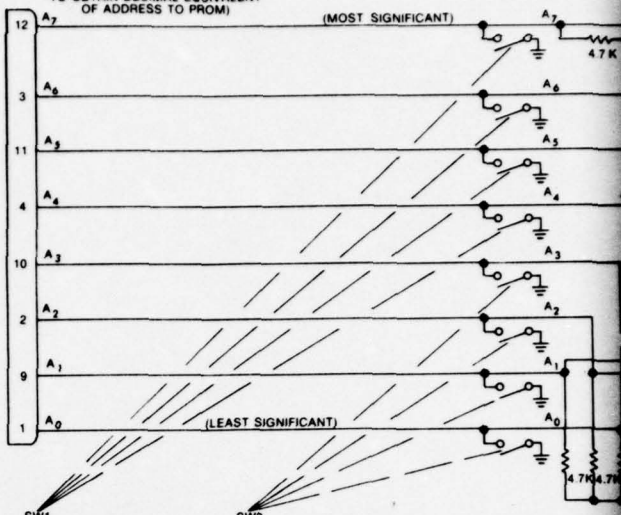


Figure 5-3. HSTCXO to Interface Adapter, Wiring Diagram.

15-SOCKET CONNECTOR
MIL PN M24308/1-2

J1 (ON PENDANT CABLE)
(PLUG INTO P1 ON 7-BIT/3 DIGIT DISPLAY
TO OBTAIN DECIMAL EQUIVALENT
OF ADDRESS TO PROM)

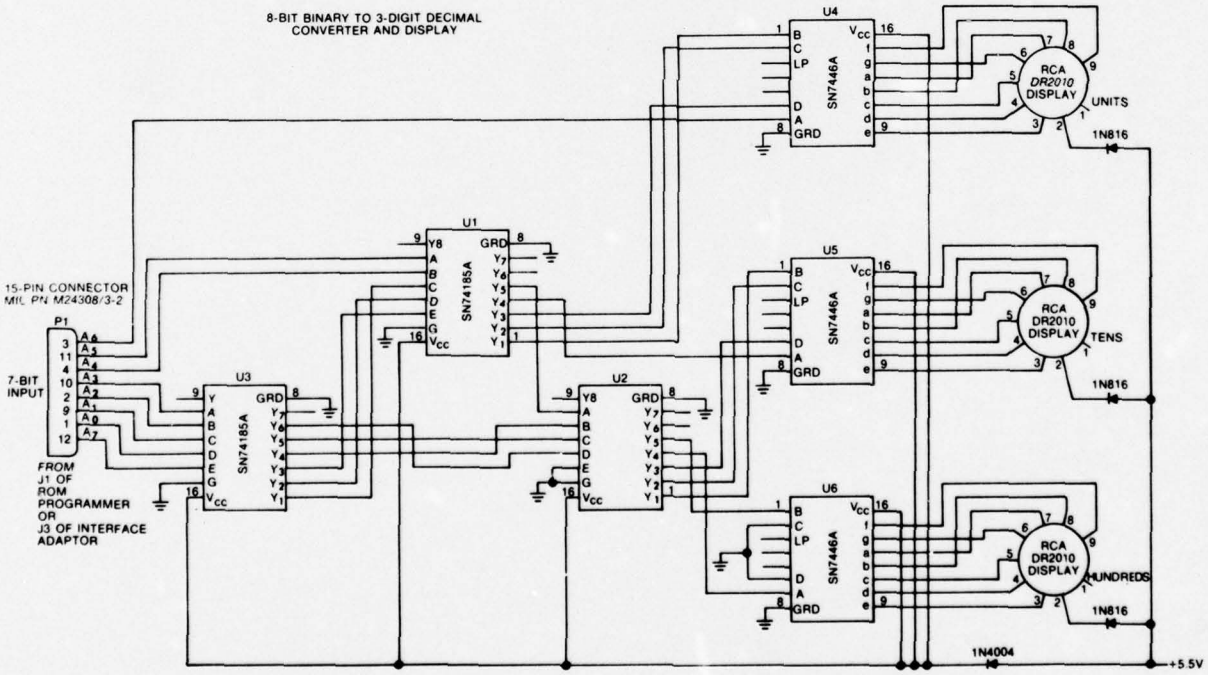


SW1
4-BIT BCD SWITCH
(CLOSE/GROUND FOR LOGIC '0',
OPEN FOR LOGIC '1')

SW2
4-BIT BCD SWITCH
(CLOSE/GRD FOR LOGIC '0',
OPEN FOR LOGIC '1')

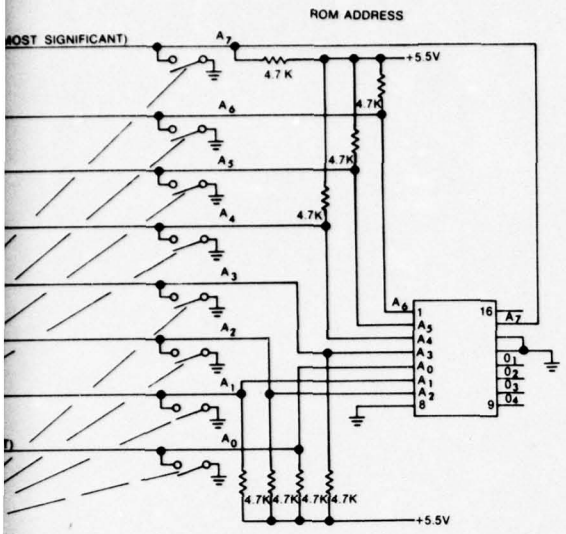
SW 1 POSITION	OUTPUT LINE A7	A6	A5	A4	SW 2 POSITION	OUTPUT LINE A3	A2	A1	A0	COMBINED DECIMAL REPRESENTATION SW1 PLUS SW2
1	0	0	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
8	1	1	1	1	16	1	1	1	1	255
DECIMAL WGT →	2^7	2^6	2^5	2^4		2^3	2^2	2^1	2^0	

8-BIT BINARY TO 3-DIGIT DECIMAL
CONVERTER AND DISPLAY



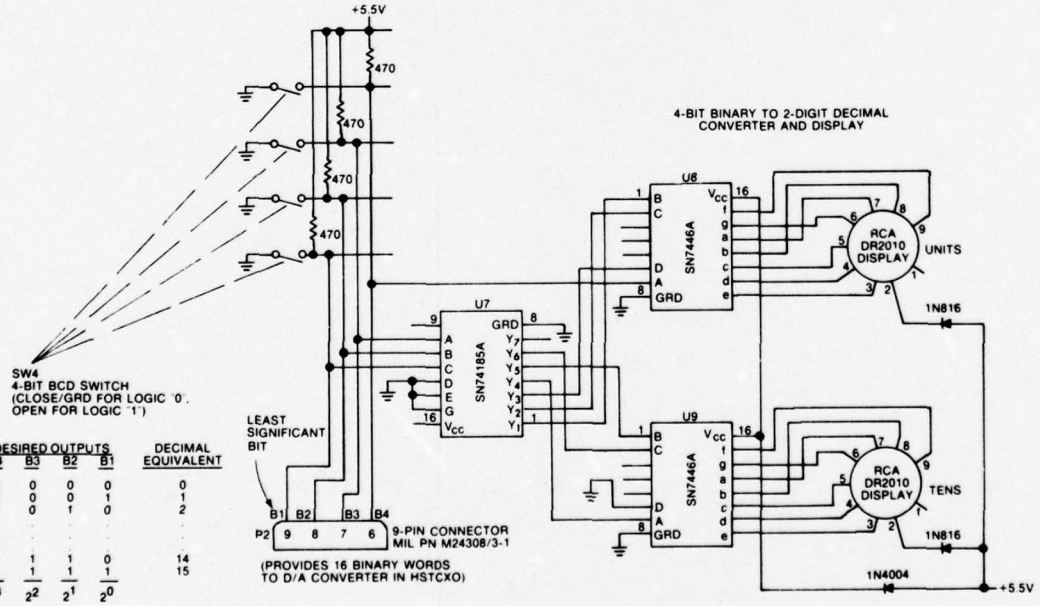
SW4
4-BIT BCD
(CLOSE/GR
OPEN FOR

SW4 POSITION	DESIRED OUT B4	B3	
1	0	0	0
2	0	0	0
3	0	0	1
.	.	.	.
.	.	.	.
15	1	1	1
16	1	1	1
DECIMAL WGTS →	2^3	2^2	2^1



ITCH
OR LOGIC '0',
GIC '1')

OUTPUT LINE			COMBINED DECIMAL REPRESENTATION SW1 PLUS SW2
A2	A1	A0	
0	0	0	0
			.
			.
			.
1	1	1	255
2^2	2^1	2^0	



SW4 POSITION	DESIRED OUTPUTS B4	B3	B2	B1	DECIMAL EQUIVALENT
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
.	.	.	.	.	.
15	1	1	1	0	14
16	1	1	1	1	15
DECIMAL WGTS →	2^3	2^2	2^1	2^0	

Figure 5-4. HSTCXO Test Fixture/PROM Programmer, Schematic Diagram.

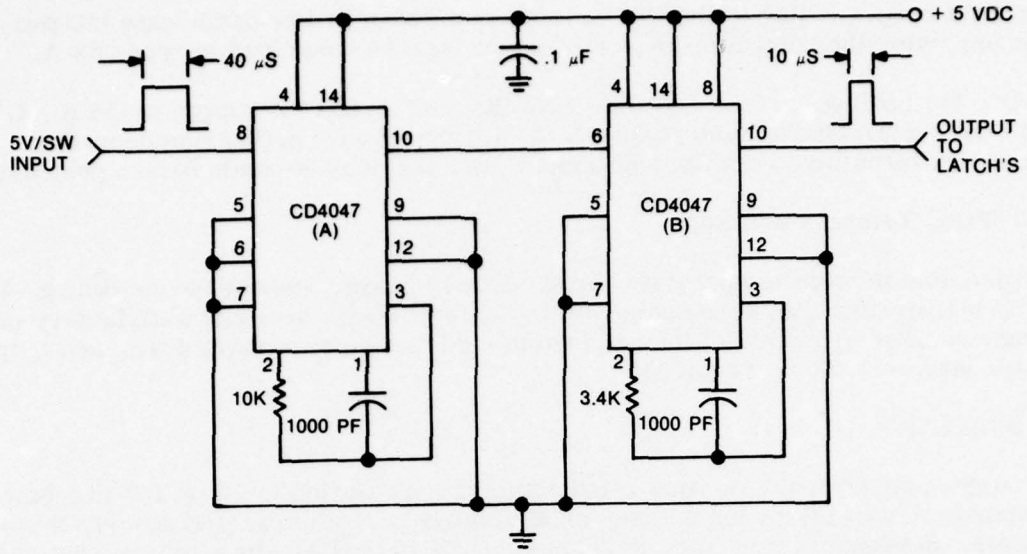


Figure 5-5. Monostable Multivibrator for Interface Adapter.

With ROM output word set at number 7 on the test fixture, complete coarse compensation to ±4 pp 10^7 maximum, from -46 to +85 °C, using conventional techniques.[6] At the same time, refine the selection of resistors R201 and R202. Disconnect decade boxes and install resistors of equal value for R101, R102, and R103, Use two resistors in series to obtain desired values, if necessary. Seal the cover on the coarse tcxo in preparation for fine compensation. (Alternately, the quality of resistor selection may be determined by an extra temperature run prior to fine compensation.)

5.2 FINE COMPENSATION

5.2.1 Initial Temperature Run

Stabilize the unit at room temperature for 10 hours minimum. Beginning at -46 °C, stabilize the sealed, coarsely compensated tcxo in 4 or 5 °C intervals up to +85 °C. (A series of 4 °C steps can be taken as quickly as 5 °C steps, due to the smaller thermal transient.) At each temperature record the ROM address, measure output frequency for ROM output word #7 (that is, verify coarse compensation), and record the decimal number of the ROM output word that produces the smallest frequency error.

5.2.2 ROM Programming

Tabularize the recorded ROM addresses and the desired corresponding output words. Use the HSTCXO computer program to obtain the intermediate ROM addresses by linear interpolation. (That is, if output words 8 and 3 were found required at addresses 107 and 112, respective intermediate interpolations are: 7 at 108, 6 at 109, 5 at 110, and 4 at 111.)

Automatic programming of the PROM is accomplished by use of the data I/O programmer using the computer-generated paper tape as described in appendix A.

Remove the cabling harness from the HSTCXO and install the programmed ROM. Clean the circuit boards, and postcoat. Attach cover over digital compensation boards. (Alternately, a confirming temperature run may be made before postcoating.)

5.2.3 Final Temperature Run

Stabilize unit at room temperature for at least 10 hours. Repeat the preceding -46 to +85 °C temperature run at the same 4 or 5 °C increments to verify satisfactory performance. Measurements of load and voltage coefficients, current drain, and output voltage may be made as required.

5.3 SUMMARY

The number of temperature runs required for compensation to ±5 pp 10^8 is a function of experience as well as consistency of component parameters, particularly those of crystals. Reasonable expectations should be 4 to 10 partial temperature runs (2 to 4 temperatures each, either below or above room temperature) and 2 to 3 full temperature runs (31 temperatures each, at 4 °C intervals).

Equipment and test fixtures described in section 5 were used to compensate and test fabricate HSTCXO models. A summary of test data follows, along with explanatory comments.

6.1 F-T CHARACTERISTICS (STATIC)

The static F-T characteristics of the five HSTCXO's, measured in 4 °C steps, are shown in figures 6-1 through 6-5. HSTCXO No 3 shows two frequency readings out of specification. This was due to a defective ladder resistor chip in the digital package. HSTCXO No 4 shows a frequency reading out of specification at -46 °C; this error was caused by recording PROM address at -45 °C instead of -46 °C.

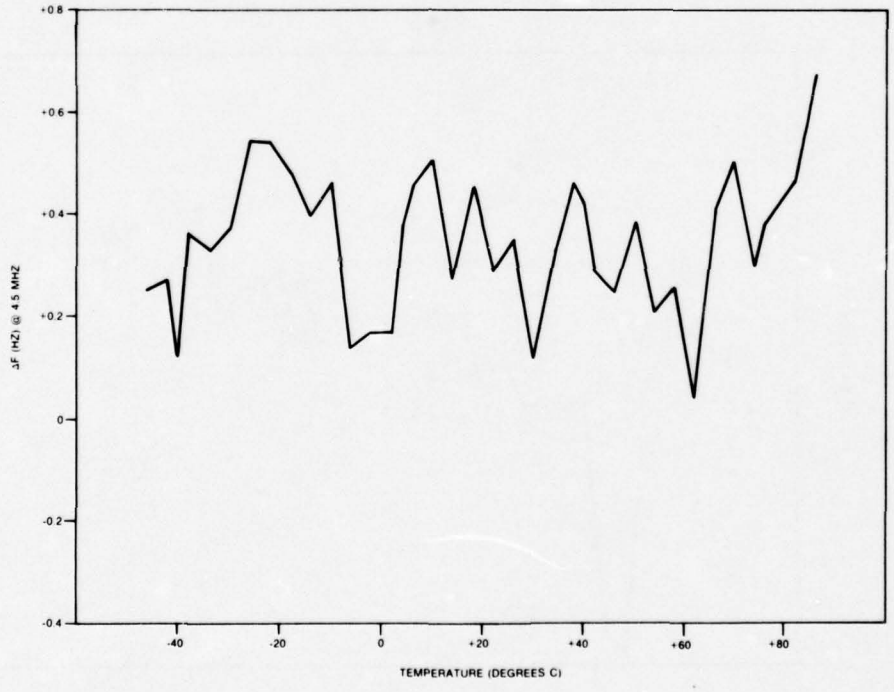


Figure 6-1. F-T Characteristics of HSTCXO Model SN-1 (Static).

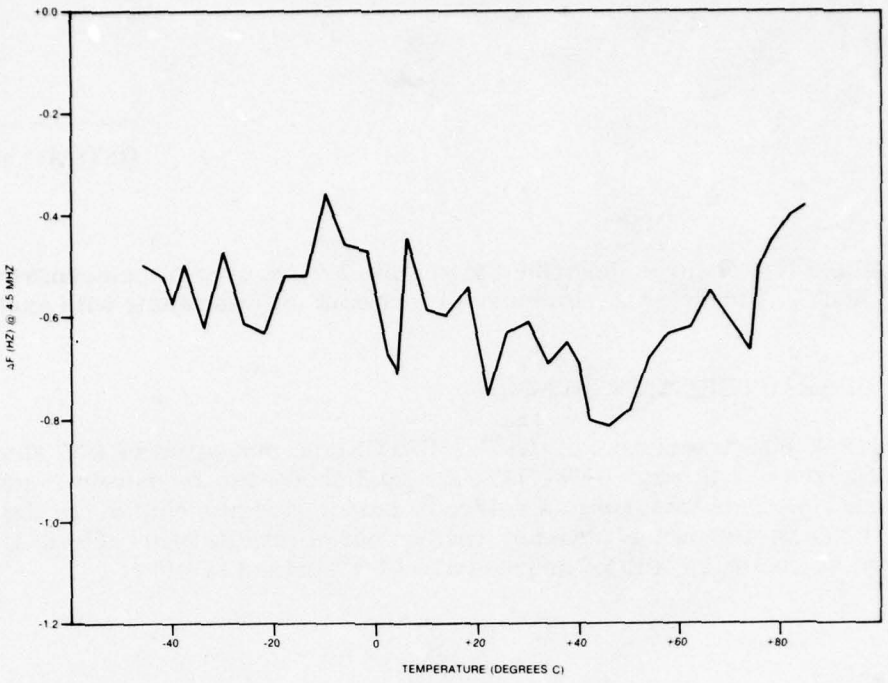


Figure 6-2. F-T Characteristics of HSTCXO Model SN-2 (Static).

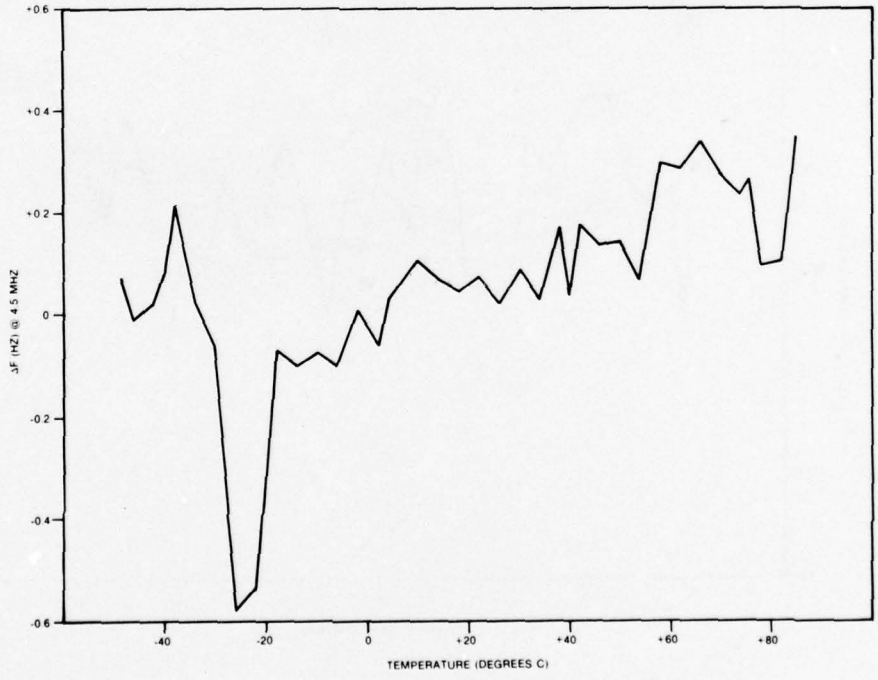


Figure 6-3. F-T Characteristics of HSTCXO Model SN-3 (Static).

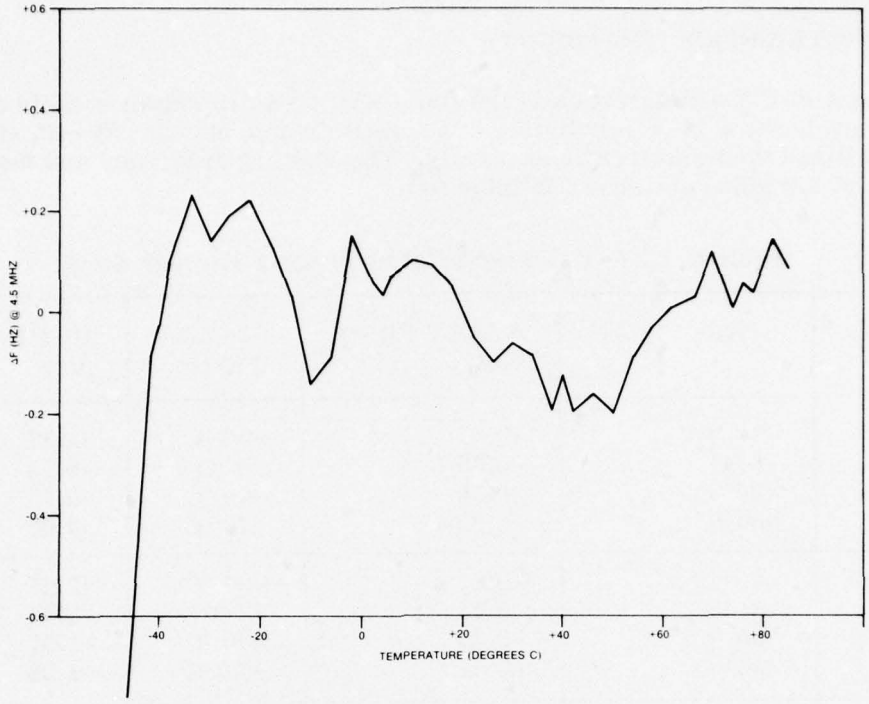


Figure 6-4. F-T Characteristics of HSTCXO Model SN-4 (Static).

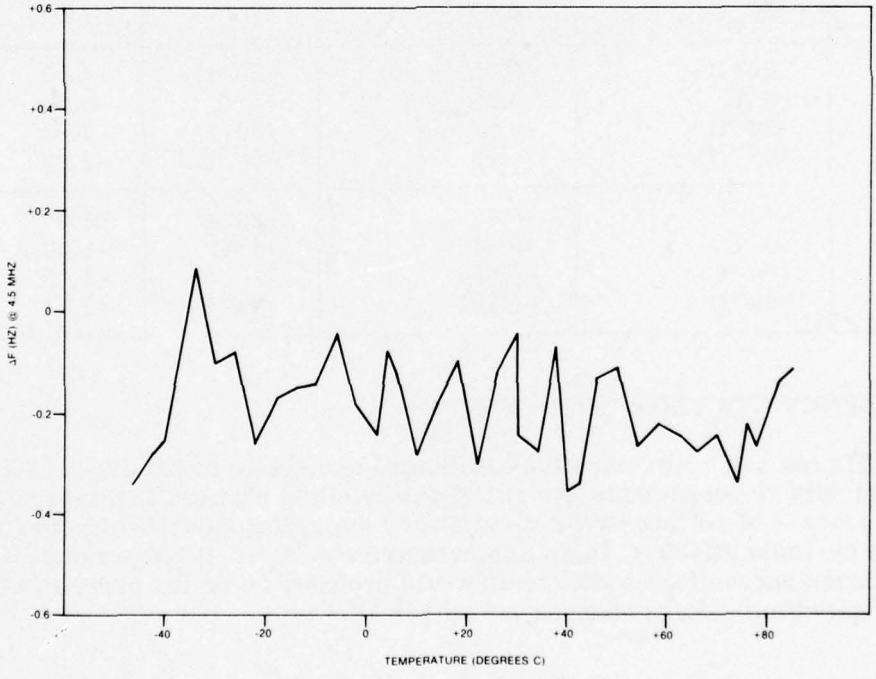


Figure 6-5. F-T Characteristics of HSTCXO Model SN-5 (Static).

6.2 CHARACTERISTICS (TRANSIENT)

The transient F-T characteristics of the five HSTCXO's are shown in table 6-1. These runs were made for a 10 °C amplitude, 1 °C/minute ramp, starting at -40, -6, +30, and +66 °C stabilized temperatures respectively. The starting frequency and the 10-minute frequency, at 4.5 MHz, are shown in table 6-1.

Table 6-1. F-T Characteristics of SN-1 Through SN-5.

HSTCXO NO	START TEMP	START FREQ (Hz)	10-MIN TEMP	10-MIN FREQ (Hz)
SN-1	-40 °C -6 °C +30 °C +66 °C	+0.47 -0.35 +0.50 +0.85	-30 °C +4 °C +40 °C +76 °C	+1.37 -0.14 -0.45 +0.06
SN-2	-40 °C -6 °C +30 °C +66 °C	-0.62 -0.35 -0.54 -0.44	-30 °C +4 °C +40 °C +76 °C	+2.27 -1.41 -1.97 -1.28
SN-3	-40 °C -6 °C +30 °C +66 °C	-0.18 -0.35 -0.19 -0.05	-30 °C +4 °C +40 °C +76 °C	+0.54 -1.04 -1.59 -1.04
SN-4	-40 °C -6 °C +30 °C +66 °C	+0.39 +0.22 +0.21 +0.25	-30 °C +4 °C +40 °C +76 °C	+1.53 -0.56 -1.09 -1.67
SN-5	-40 °C -6 °C +30 °C +66 °C	+0.67 +0.46 -0.06 -0.29	-30 °C +4 °C +40 °C +76 °C	+1.67 -0.47 -1.19 -1.14

6.3 FREQUENCY-VOLTAGE COEFFICIENTS

Voltage coefficients of representative oscillators are shown in table 6-2. Some of the apparent voltage coefficients are really due to slight changes in temperature during the process of setting power supplies and recording data, despite the attempt to maintain the units at +30 °C in the temperature chamber. If temperature drifts were subtracted out, voltage coefficients would probably be on the order of ±1 pp 10^9 or less for specified voltage changes (±5 pp 10^9 allowed).

Table 6-2. Frequency-Voltage Coefficients.

SERIAL NO	FREQUENCY CHANGE IN PP 10^{10} FROM STANDARD +10-V DC CONDITIONS		
	9.50 V	10.00 V	10.50 V
1	0	0	0
2	-4	0	0
3	-2	0	0
4	-2	0	0
5	0	0	+4

6.4 FREQUENCY-LOAD COEFFICIENTS

Frequency changes caused by changes in load impedance were measured with a load box calibrated with an HP 4815A rf vector impedance meter. In addition to stabilizing HSTCXO models at +30 °C, loads were quickly changed by a selector switch to minimize temperature drift during measurement. Data for representative models is shown in table 6-3, indicating the load coefficients are less than 1 pp 10^9 total change for very large load changes. The specified limit was ±5 pp 10^9.

Table 6-3. Frequency-Load Coefficients.

SERIAL NO	CHANGE IN FREQUENCY IN PP 10^{10} FOR SPECIFIED LOADS					
	OUTPUT A			OUTPUT B		
	45 Ω	50 Ω	55 Ω	25 pF	30 pF	35 pF
1	-1	0	+2	+20	0	-20
2	-8	0	+8	-20	0	+20
3	-2	0	+1	0	0	0
4	-8	0	+6	-3	0	+3
5	-8	0	+4	-4	0	+4

6.5 RF OUTPUT LEVELS

Output levels, measured at room temperature with specified loads, are summarized in table 6-4.

Table 6-4. RF Output Levels.

SERIAL NO	OUTPUT A (50-OHM LOAD)	OUTPUT B (30-pF LOAD)
1	129 mV	.450 9.1 V
2	.310 123 mV	.440 9.0 V
3	.365 115 mV	.380 9.0 V
4	.385 125 mV	.400 9.0 V
5	106 mV	.390 9.0 V

6.6 POWER DISSIPATION

Current drain required by representative models was measured for nominal supply voltages of +10. Results were quite consistent and easily satisfied the 100-mW-maximum specification. Refer to table 6-5.

Table 6-5. Power Dissipation Measurements.

SERIAL NO	TEMPERATURE	CURRENT DRAIN (mA) FOR +10 V DC	TOTAL POWER (mW)
1	+30 °C	8.0	84.00
2	+30 °C	7.0	73.50
3	+30 °C	7.9	82.95
4	+30 °C	8.5	89.25
5	+30 °C	6.8	71.40

6.7 WARMUP TIME

Table 6-6 shows the warmup characteristics of five oscillators after they were stabilized (unoperating) for approximately 45 minutes at +30 °C in a temperature chamber. Frequency within 1 minute was not within ±1 pp 10^8 because the frequency was not reset to 4.5 MHz prior to warmup run.

Table 6-6. Warmup Characteristics.

SERIAL NO	FREQUENCY IN PARTS 10^8 OF FINAL FREQUENCY	
	TIME, START	TIME, 1 MINUTE
1	+69.5	+8.6
2	+38.0	-1.7
3	+79.0	-3.1
4	+24.7	-2.4
5	+44.2	+2.2

6.8 FREQUENCY ADJUSTMENT

Table 6-7 shows the minimum and maximum frequencies of the five HSTCXO's as obtained by adjustment of the trimmer, C106. Since positive aging should take place, most of the available trim range is used to lower the 4.5-MHz output frequency.

Table 6-7. Frequency Adjustment Range.

SERIAL NO	FREQUENCY IN PARTS 10^6	
	TRIMMER MINIMUM	TRIMMER MAXIMUM
1	+0.63	-2.39
2	+1.42	-2.33
3	+1.69	-1.69
4	+0.51	-2.61
5	+0.17	-2.25

6.9 NOISE MEASUREMENTS

For information, signal-to-noise ratio measurements were made on five HSTCXO models, using a Collins 876H-1 Carrier Suppressor and Spectrum Analyzer. The carrier suppressor is essentially a very narrow, tunable notch filter that permits at least 60-dB suppression of the carrier, then 60-dB reamplification of both noise and suppressed carrier, in order to extend the effective dynamic range of the spectrum analyzer to 120 dB. The technique and equipment have been described previously in the literature.[14] Figures 6-6 through 6-8 show the results.

6.10 RETRACE CHARACTERISTICS

Retrace runs were made on the five engineering models. Included in this section is earlier data pertaining to the retrace problem.

Table 6-8 shows measured data on the five HSTCXO models when subjected to the specified temperatures and times. The design goal of ±3 pp 10^8 (or ±0.135 Hz) was not met for all of the temperatures called out.

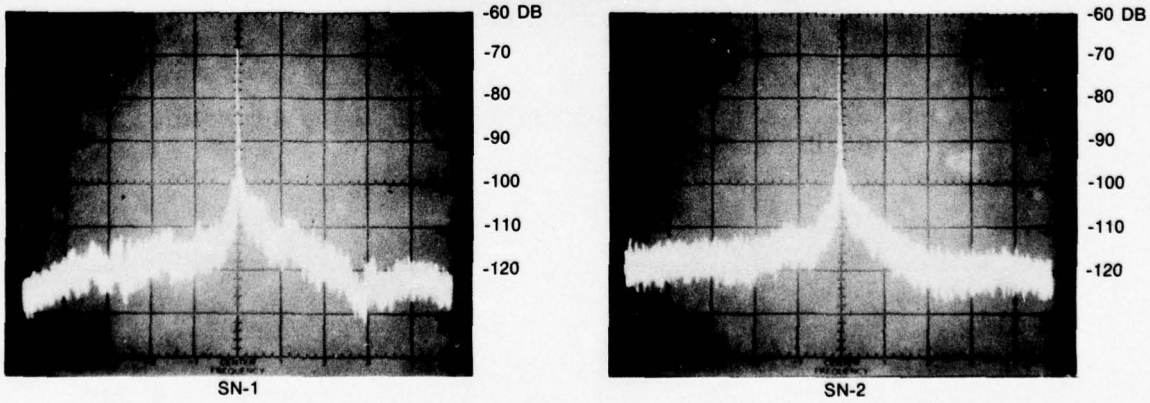


Figure 6-6. S/N Measurement (Carrier Suppressed and Reamplified 60 dB), Models SN-1 and SN-2.

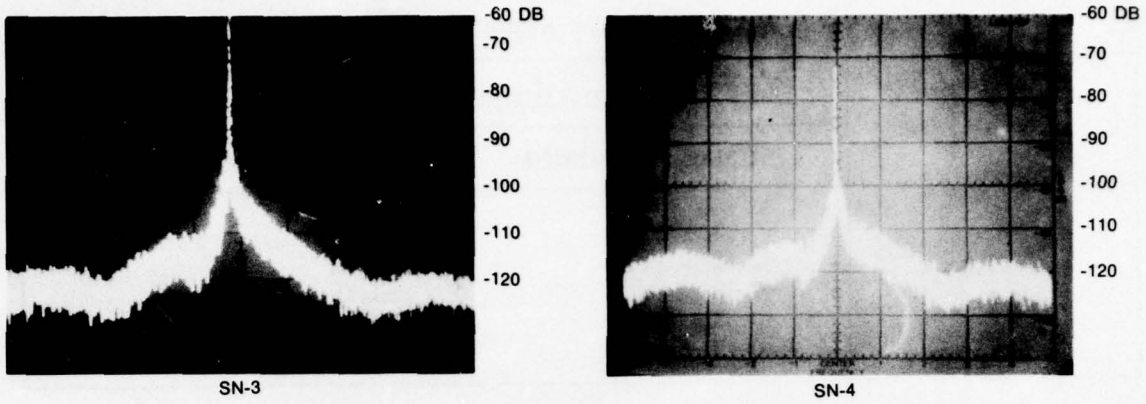


Figure 6-7. S/N Measurement (Carrier Suppressed and Reamplified 60 dB), Models SN-3 and SN-4.

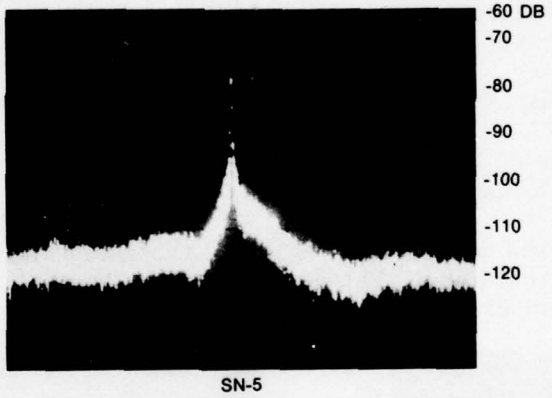


Figure 6-8. S/N Measurement (Carrier Suppressed and Reamplified 60 dB), Model SN-5.

Table 6-8. Frequency-Temperature Stability (Hz) at 4.5 MHz (Retrace).

TEMP	TIME	FREQ NO 1	FREQ NO 2	FREQ NO 3	FREQ NO 4	FREQ NO 5
-57 °C	16 hr	Storage	Storage	Storage	Storage	Storage
-46 °C	1.9 hr	+0.86	+0.15	-0.88	+0.09	-0.28
-30 °C	1.5 hr	+0.51	-0.54	+0.28	-0.07	+0.31
+85 °C	1.5 hr	-0.20	-0.75	+0.18	-0.41	-0.08
-46 °C	1.5 hr	-0.22	-0.77	-0.98	-2.07	-1.46
+85 °C	1.5 hr	+0.13	-0.58	+0.22	-0.23	+0.04
+30 °C	1.5 hr	+0.75	-0.20	+0.61	+0.73	+0.61

Frequency-temperature stability and frequency-temperature retrace are all functions of a phenomenon commonly referred to as "crystal hysteresis," or the failure of a crystal to return repeatedly to the same frequency at a given temperature if the prior temperature variations are different. As the whole theory of temperature compensation is based on providing previously determined frequency corrections at given temperatures, the corrections will be in error by the amount the crystal fails to retrace. Also, another source of error in table 6-8 may be attributed to resettability of the temperature chamber used to log the frequency data.

The problem of crystal hysteresis has been known for some time and was recognized in both of the previous development contracts. The first development contract, DAAB07-71-C-0136, specified frequency-temperature retrace only under identical conditions -- prior stabilization temperature and time, rate of change of temperature to the starting point, starting temperature and stabilization time, and rate of change during the frequency-temperature test. The second development contract, DAAB07-73-C-0137, is for the purpose of miniaturization and further investigations into hysteresis, thermal transient response, aging, and simplification of the compensation technique. The actual frequency-temperature stability specification remained the same as on the first contract.

It has been our experience on the development contracts that crystal suppliers will not commit themselves to a firm specification on crystal frequency retrace, insisting instead on best-effort clause. It has also been our experience that few of the crystals received met the $\pm 3 \times 10^{-8}$ retrace requirement of paragraph 1.3.4 of the technical guidelines dated 28 March 1974.

While considering why crystal data might be exaggerated, it was observed that the same type of thin-film oscillator package was in the tcxo described in figure 3-2 and in the oscillator used to obtain cyrstal retrace data (table 4-4 and figure 4-31). Further study revealed that class II ceramics, usually used in high-capacitance bypass capacitors, exhibit capacitance changes with time and temperature very similar in profile to frequency retrace errors measured in crystals. Capacitance changes are exponential with time, are temperature dependent, and are normally experessed as percent capacitance change per unit of time (such as -2 percent/decade).[12] The time zero reference is the last exposure to a temperature in excess of 125 °C where de-aging is nearly complete; exposure time to lower temperatures, where aging begins again, is expressed in hours. Typical room temperature aging rates of class II ferroelectric ceramics are -1.5, -2.0, and -4 percent/decade for dielectric constants of 700, 2,000, and 8,000 respectively.[15] It therefore seems possible that bypass capacitors may be at least contributing to tcxo retrace errors. Note, for example, that the first 2-percent decrease in capacitance (corresponding to a rise in oscillator frequency) occurs in the

first 10 hours after high temperature exposure, but it takes another 90 hours to decrease another 2 percent.

The similarity of capacitor aging and crystal retrace characteristics (figure 4-31) is interesting but not definitely interdependent. That is, investigation into components and the type of substrate used in the thin-film oscillator package revealed only one class II bypass and that was from B+ to ground; all other materials are class I, typically found in tc capacitors, that do not exhibit the rapid aging characteristic of class II materials. Further doubt is reflected on capacitors causing retrace errors in crystals by observing that both retrace measurements methods, the VVM and the Pierce oscillator, yielded similar results (table 4-4). The VVM crystal test set certainly did not use class II ceramic capacitors in the pi network.

Conclusions

Successful design, construction, and operation of the 2-cubic-inch HSTCXO's have been demonstrated using digital compensation. Stabilities of ±5 pp 10^8 have been obtained from -46 to +85 °C. A single power supply of +10 V dc supplied both the coarse and digital circuitry with a power drain of less than 100 milliwatts. Since the components used are small and the thin-film parts much smaller, the shock and vibration characteristics are excellent for high-reliability communication equipment, including space applications.

There are two limiting factors that tend to make frequency compensation to less than 5 parts in 10^8 impractical. One is thermal hysteresis in the quartz crystal itself. At the present, selection is made from twenty crystals to choose units with the lowest frequency retrace error at the lower turning point. The other is thermal transients which, in a small volume such as the HSTCXO, are difficult to control, for there is no space available for thermal insulation. To use the HSTCXO in environments where temperature transients may be as high as 5 to 10 °C/minute, external insulation would be required.

High volume production cost estimates seem to be compatible with oven-controlled oscillators with equal stability requirements. The long-term aging should be compatible or better than oven crystal oscillators, since the crystal would see a lower ambient temperature most of its life.

Literature Cited

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Appendix A

Computer Program for PROM Using Tape Printout

DIGCMP is a computer program in FORTRAN to automatically interpolate the temperature correction coefficients for the oscillator. The input to the program is a set of data point measurements of temperature, corresponding address, and correction word for the given temperature. (These are denoted by TEMP, ADD, and NCW, respectively, in the program.)

In the PROM (programmable read only memory), U202, which utilizes this program's output, only integer addresses are used. Therefore, the lowest and highest integers (ILOW and IHIGH) in the interpolation range are calculated. The interpolation procedure uses linear interpolation to find TEMP, ADD, and NCW for every integer address from ILOW to IHIGH.

The data for PROM addresses outside actual data input are set to the values computed for ADD = IHIGH. The program then allows any output data point to be modified manually by specifying the number of such corrections to be made (NCORR) and the new temperature, address, and correction words (TEMPC, IADDC, and NCWC respectively).

DIGCMP builds a generalized PROM data file on mass storage. A second program, PROMOO, accepts the data from the mass storage file as well as input directives which describe the polarity, number of parallel bits, and number of words in the PROM to be programmed. The output of PROMOO is processed through a paper tape interface routine which builds the final paper tape file on mass storage. This paper tape file is then directed to an RJE terminal which actually punches paper tape (figure A-1) suitable for loading the data I/O PROM programmer.

Figure A-1. Paper Tape Used in the Data I/O PROM Programmer.

```
@RUN,C  DIGCMP,89817101,055360,002,50 . DON MOOTY                    CA079

@ASG,A   PAPERTAPE.

@USE  PT.,PAPERTAPE

@USE U.,NEW*UTEX29.

@ASG,AX U.

@ASG,AX DIGC'P.

@USE DG.,DIGCMP.

@DELETE,C  PFILE.
FURPUR 27R1C RL71-A 03/26/78 17:21:08

@ASG,UP  PFILE.F
```



```
@ELT,L DG.SER3,DG.SER3
ELT017 RL1870 03/26-17:21:04-(0,0)
000001      000     $LAT1N IFMP=-36.5,-38,-42,-46,-47,-47,-45,-45,-78,-74,-70,-66,-62,-58,-54,-50,
000002      000     46,42,38,34,30,26,22,18,14,10,6,2,-2,-6,-10,-14,-18,-22,-26,-30,-34,-37,
000003      000     -48.,-60.,
000004      000     ALD=0.,3.25,7.5,12.75,25,40,42.25,56.5,57.5,64,70,75,78.75,83.25,  5,
000005      000     94.75,100.5,107.25,112.75,118.75,124.25,130.25,137.25,142.75,148.25,156.5,
000006      000     162.75,170,177.25,185.25,193.25,201,208.75,217.25,224,232.75,239.5,249.75,
000007      000     255.,27,25,37.,
000008      000     NCW=15,15,14,13,11,8,7,3,0,0,0,1,3,5,7,9,10,12,13,14,14,14,14,14,
000009      000     12,12,12,12,11,11,12,12,13,14,15,15,15,15,14,,

END ELT.
```

```
@CR*DA.IFT,IRS DG,DIGCMP
IFT L2.3
ON 26 MAR 76 AT 17:21:44  CYCLE  (,0)


NO. (..)=NESTING DEPTH

  1       C  **  LPROM MUST BE SET TO THE WORD LENGTH OF THE PROM
  2              PARAMETER LPROM=256
  3       C  **  ND MUST BE SET TO THE NUMBER OF INPUT DATA POINTS
  4              PARAMETER ND=50
  5              PARAMETER NDE=ND*(ND+1)/2,NC=ND/2
  6              REAL NCW2
  7              DATA IMAX/2/
  8       C
  9       C      NOTE XNEW1 SHOULD NOT BE USED FOR ERROR INTERPOLATION
 10       C      MAX NCW SET FOR 2ND ORDER FIT
 11              LOGICAL D                                              ; DEBUG
 12             $ F                                                     ; COMPLEX
 13              DIMENSION ID(2)/2*' '/
 14              REAL RADD(LPROM),NCW(LPROM)
 15              DIMENSION TEMP(LPROM),ADD(ND),NCW(LPROM),IF(2,2),
             $ ADD2(ND),
 16             $ NCW2(ND),DELADD(NDD),DELTEMP(NDE),IALOC(NC),SLOPE(NC),
             $ NCWC(NC)
 17              NAMELIST/DATIN/ITEMP,ADD,NC,IMAX,NCORR,IF,NC,IALOC,
             $ NCWC
 18       C  **  NCORR IS THE NUMBER OF CORRECTIONS TO BE APPLIED CURRENTLY AVAILABLE
 19       C  **  TEMPC IS THE CORRECTION VECTOR FOR THE REFERENCE DATA
 20       C  **  IALOC IS THE ADDRESS CORRECTION VECTOR FOR SPECIFIED TEMPERATURE
 21       C  **  NCWC IS THE NCW CORRECTION VECTOR CORRESPONDING TO TEMPC AND IALOC
 22              CALL OPTSW(LOPTS)                                      ; GET OPTIONS
 23              D=FLD(4+IBP,1,LOPTS).EQ.1
 24              F=FLD(4+IBP,1,LOPTS).EQ.1
 25              NCORR=0
 26              NUMADD=LPROM
 27              READ(5,DATIN)
 28       C          CORRECT FOR DISCREPANCY IN SPECIFIED DATA POINT COUNT
 29              NPTS=ND
 30              DO 121 IL=1,ND
 31              IK=ND+1-IL
 32              IF(ITEMP(IK).EQ.0.OR.ADD(IK).EQ.0.OR.NCW(IK).EQ.0) GO
             $ TO 122
 33              NPTS=NPTS-1
 34       121    CONTINUE
 35       122    CONTINUE
 36              PRINT 62
 37       70     WRITE(6,61)
 38       61     FORMAT(' INPUT DATA'//)
 39              CALL HED829('TEMP','ADDRESS','NCW',NB,NB,NB,NB)
 40              WRITE(6,64)
 41              DO 22 ITEM=1,NPTS
 42              CALL PRT829(TEMP(ITEM),ADD(ITEM),NCW(ITEM),IF,NB,NB,
             $ NB,NB)
 43       22     CONTINUE
```

```
NO. (..)=NESTING DEPTH

                WRITE(6,62)
        62      FORMAT(1H1)
        64      FORMAT(//)
        C           PUT ADDRESS DATA IN MONOTONE INCREASING ORDER
                MAX=1.E8
                DO 23 IT=1,NPTS
                MIN=1
                DO 24 I=2,NPTS
                IF(ADD(I).LT.ADD(MIN)) MIN=I
        24      CONTINUE
                TEMP2(IT)=TEMP(MIN)
                ADD2(IT)=ADD(MIN)
                NCW2(IT)=NCW(MIN)
                TEMP(MIN)=MAX
                ADD(MIN)=MAX
                NCW(MIN)=MAX
        23      CONTINUE
        C   ** ILOW AND IHIGH SPECIFY THE INTEGER RANGE OF INPUT DATA FOR REGULA
                ILOW=1 +ADD2(1)                                  ! SUBSCRIPT = ADDRESS+1
                IHIGH=ADD2(NPTS) +1
                IF(L)                                            ! DEBUG
     ( 1)          PRINT 1000
     ( 1)  1000    FORMAT('1REARRANGED DATA')
     ( 1)          CALL HEADER('TEMP    ','ADDRESS','NCW    ',W,L,
        ( 1)     $    PE,LABLE )
     ( 1)          DO (ITEM=1,NPTS)
     ( 2)             CALL PRINT2(TEMP2(ITEM),ADD2(ITEM),NCW2(ITEM),
        ( 2)     $       L,PE,'E',PE)
     ( 1)          END DO ( 10)
                END IF ( P4)
        C   **  PRINT INPUT DATA INFORMATION
                PRINT 62
                PRINT99,NPTS,ILOW,IHIGH
        99      FORMAT(' NPTS=', I10,5X,'ILOW=', I10,5X,'IHIGH=',
               $ I10//)
        C   ** SET UP DIVIDED-DIFFERENCE TABLE  **
                CALL DDTAB(ADD2,NCW2,NPTS,MAX,DDADD)
                CALL DDTAB(ADD2,TEMP2,NPTS,MAX,DDTEMP)
        C   **  INTERPOLATE ADDRESS AND TEMPERATURE
                IF(L)                                            ! DEBUG
     ( 1)          PRINT 1020
     ( 1)  1020    FORMAT(' DIVIDED DIFFERENCE TABLE')
     ( 1)          PRINT 1010,(KKK,ADD2(KKK),DDADD(KKK),DDADD(NPTS+
        ( 1)     $    KKK),
     ( 1)     $    DDADD(2*NPTS-1+KKK),KKK=1,NPTS)
     ( 1)          PRINT 1020
     ( 1)          PRINT 1010,(KKK,ADD2(KKK),DDTEMP(KKK),DDTEMP(NPTS+
        ( 1)     $    KKK),
     ( 1)     $    DDTEMP(2*NPTS-1+KKK ),KKK=1,NPTS)
     ( 1)  1010    FORMAT(I5,4F10.4)
                END IF ( P0)
                DO 44 J=ILOW,IHIGH
                X=J-1                                            ! ADDRESS = SUBSCRIPT -1
                RNCW(J) = XNEWT(X,MAX,ADD2,DDADD,NPTS,MAX)
                NCW(J) = .5+RNCW(J)
```

```
NO. (..)=NESTING DEPTH

 94              TEMP(J)=XINTRP(X,XMX,ADD2,DDTEMP,NPTS,DMY)
 95        44    CONTINUE
 96        C  **  FILL ADDRESSES OUTSIDE OF INPUT DATA RANGE
 97              IF(IHIGH.GE.LPROM) GO TO 7015
 98              IBG=IHIGH+1
 99              DO 701 ICHNG=IBG,LPROM
100              NCW(ICHNG)=NCW(IHIGH)
101              TEMP(ICHNG)=TEMP(IHIGH)
102        701   CONTINUE
103         7015 CONTINUE
104              IF(ILOW.EW.1) GO TO 702
105              IEND=ILOW-1
106              DO 703 ISCH=1,IEND
107              NCW(ISCH)=NCW(INTGH)
108              TEMP(ISCH)=TEMP(INTGH)
109        703   CONTINUE
110        C  **  MAKE CORRECTIONS SPECIFIED IN INPUT    **
111        702   IF(ICORR.EQ.0) GO TO 56
112              DO 55 JJ=1,ICORR
113              IC=IADDC(JJ)+1
114              NCW(IC)=NCC(JJ)
115              TEMP(IC)=TEMPC(JJ)
116        55    CONTINUE
117           56 CONTINUE
118        C  **  PRINT RESULTS
119              KK=1
120        71    ITAB=0
121              PRINT 62
122              WRITE(6,3)
123        63    FORMAT(' OUTPUT DATA'//)
124              WRITE(6,64)
125              CALL HEDR29('TEMP',' ADDRESS','NCW',' ',' ',' ',
                1 ' ')
126        72    K=KK-1
127              IADD(KK)=K
128              CALL PRT629(TEMP(KK),K,NCW(KK),RNCW(KK),' ',' ',' ',' ')
129              ITAB=ITAB+1
130              KK=KK+1
131              IF(KK.GT.LPROM) GO TO 801
132              IF(ITAB.LT.45) GO TO 72
133              GO TO 71
134        801   PRINT 62
135              IF(F)                                          C COMPILOT
136     ( 1)        CALL TCMP29('INTERPOLATED DATA*','NCW*','ADDRESS*
        ( 1)     1     ')
137     ( 1)        CALL PCMP29(KADD,RNCW,1,LPROM,1)
138     ( 1)        CALL TCMP29('INPUT DATA*','PNCW*','ADDRESS*')
139     ( 1)        CALL PCMP29(ADD2,NCW2,1,NPTS,1)
140              END IF ( 135)
141        C  **  GENERATE PAPER TAPE DATA FILE
142              CALL BPRM00('PFILE.','ONLY.',4)
143              DO 802 JK=1,LPROM
144              JADD=JK-1
145              CALL BPDT00(JADD,NCW(JK))
146        802   CONTINUE
```

```
NO. (..)=NESTING DEPTH

147             CALL BPCL00
148             STOP
149             END

CP TIME WAS      1.837 SECONDS
TOTAL NUMBER OF IFTRAN  STATEMENTS IS     8
TOTAL NUMBER OF FORTRAN STATEMENTS IS   114
TOTAL NUMBER OF COMMENT STATEMENTS IS    19
TOTAL NUMBER OF STATEMENTS IS           145
```

79

```
@FOR,MS IFT$,SI$,DG.LIBCMP . AUTO COMPILE
FOR SOE3-03/26/76-17:24:19 (0.)

   MAIN PROGRAM

   STORAGE USED: CODE(1) 000756; DATA(6) 007641; BLANK COMMON(2) 000006

   EXTERNAL REFERENCES (BLOCK, NAME)

     0003   OPTSN%
     0004   HED824
     0005   PRT824
     0006   UDTAB
     0007   XNEW1
     0010   TC%P24
     0011   PC%P24
     0012   BPK%00
     0013   BPLT00
     0014   BPCL00
     0015   NINTR$
     0016   NRNL$
     0017   NPRT$
     0020   NIO2$
     0021   NKBD$
     0022   NIO1$
     0023   NSTOP$
```

```
STORAGE ASSIGNMENT   (BLOCK, TYPE, RELATIVE LOCATION, NAME)

0000   007522 1000F    0000   007556 1010F    0000   007550 1020F    0001   001??? 122L    [illegible]  000040 [illegible]
0001   000127 1536     0001   000164 1666     0001   000170 1726     0001   000277 2255    [illegible]  000402 [illegible]
0001   000431 2716     0001   000447 3046     0001   000525 32??     0001   000544 443?    [illegible]  000557 344?
0001   000734 4136     0001   000570 56L      0000   007505 61F      0000   007520 62F     [illegible]  007530 [illegible]
0000   007521 64F      0001   000532 7015L    0001   000551 7021     0001   00057? 71L     [illegible]  000?23 721
0001   000667 801L     0000   007537 99F      0001   000725 99990    0001   000443 99992L  [illegible]  000300 [illegible]
0001   000320 99998L   0000 R 001471 AID      0000 R 002235 A???     0000 L 00???? ?     [illegible]  007453 [illegible]
0000 R 002317 DDADD    0000 R 004712 DETEMP   0000 I 007305 IA???   0000 I 007440 INC   0000 I 007445 IC
0000 I 007441 ICHNG    0000 I 007442 TEMP     0000 I 007472 IHIGH   0000 I 007425 IR    0000 I 007424 II
0000 I 007431 ILOW     0000 I 007443 ISCH     0000 I 007447 ITAP    0000 I 00742? IT?   0000 I 007434 19999?
0000 I 007433 199996   0000 I 007436 J        0000 I 00745? JA??    0000 I 007444 JJ    0000 I 007451 J?
0000 I 007450 K        0000 I 007446 KP       0000 I 007435 KPK     0000 I 000000 MAX   0000 I 000001 [illegible]
0000 I 007430 N        0000 I 000067 NP       0000 I 007420 NCORR   0000 I 001563 NCX   0000 I 007367 [illegible]
0000 R 000002 NCK2     0000 I 000064 NMX      0000 I 007421 NOPTS   0000 I 007423 NPTS  0000 I 007427 [illegible]
0000 I 007422 NUMADD   0000 I 000066 P        0000 R 000071 RADD    0000 R 000471 RNCX  0000 R 001071 TEMP
0000 R 007336 TEMPC    0000 R 002153 TEMP2    0000 R 007437 X       0007 R 000000 XMEAN
```

```
00100        1*       C  ** LPROM MUST BE SET TO THE WORD LENGTH OF THE PROM                    000000
00101        2*             PARAMETER LPROM=256                                                  000000
00103        3*             STOP EDIT SOURCE @ ***INT. GENERATED***                              000001
00103        4*       C  ** ND MUST BE SET TO THE NUMBER OF INPUT DATA POINTS                   000001




     END OF COMPILATION:          NO  DIAGNOSTICS.

@PACK,P DG.
FURPUR 27R1C RL71-3 03/26/76 17:24:29
END PACK. TEXT=20,TOC=2,SYM=5,RFL=2,ABS=1



@MAP,IN  DG.DIGCMPMAP,DG.DIGCMP
MAP28R1 RL71-3 03/26/76 17:24:36 (,0)
END MAP

@XQT,DP DG.DIGCMP
```

INPUT DATA

TEMP	ADDRESS	FLOW
-36.5000	0	15
-38.0000	3.25000	15
-42.0000	13.2500	14
-46.0000	22.7500	12
-47.0000	25.0000	11
87.0000	40.0000	8
86.0000	42.2500	7
82.0000	50.5000	6
78.0000	57.5000	6
74.0000	64.0000	6
70.0000	70.2500	5
66.0000	76.7500	4
62.0000	83.2500	3
58.0000	89.0000	3
54.0000	94.7500	2
50.0000	100.500	2
46.0000	107.250	1
42.0000	112.750	1
38.0000	118.750	1
34.0000	124.250	15
30.0000	130.250	14
26.0000	136.250	14
22.0000	142.750	13
18.0000	149.250	14
14.0000	156.500	12
10.0000	162.750	12
6.00000	170.000	12
2.00000	177.250	12
-2.00000	185.250	11
-6.00000	193.250	11
-10.0000	201.000	12
-14.0000	208.750	12
-18.0000	216.250	13
-22.0000	224.000	14
-26.0000	232.750	15
-30.0000	239.250	15
-34.0000	249.750	15
-36.0000	255.000	15
-48.0000	27.2500	11
88.0000	38.0000	8

REORDERED DATA

TEMP	ADDRESS	NEW
-36.5000	0	15.0000
-38.0000	3.25600	15.0000
-42.0000	13.2500	14.0000
-46.0000	22.7500	12.0000
-47.0000	25.0000	11.0000
-48.0000	27.2500	11.0000
88.0000	30.0000	8.00000
87.0000	40.0000	8.00000
86.0000	42.2500	7.00000
82.0000	50.5000	5.00000
78.0000	57.5000	6
74.0000	64.0000	6
70.0000	70.2500	6
66.0000	76.7500	1.00000
62.0000	83.2500	5.00000
58.0000	89.0000	5.00000
54.0000	94.7500	7.00000
50.0000	100.500	9.00000
46.0000	107.250	10.0000
42.0000	112.750	12.0000
38.0000	118.750	13.0000
34.0000	124.250	14.0000
30.0000	130.250	14.0000
26.0000	136.250	14.0000
22.0000	142.750	14.0000
18.0000	149.250	14.0000
14.0000	156.500	12.0000
10.0000	162.750	12.0000
6.00000	170.000	12.0000
2.00000	177.250	12.0000
-2.00000	185.250	11.0000
-6.00000	193.250	11.0000
-10.0000	201.000	12.0000
-14.0000	208.750	12.0000
-18.0000	216.250	13.0000
-22.0000	224.000	14.0000
-26.0000	232.750	15.0000
-30.0000	239.250	15.0000
-34.0000	249.750	15.0000
-36.0000	255.000	15.0000

NMTS= 40 ILOW= 1 THIGH= 256

DIVIDED DIFFERENCE TABLE

1	.0000	15.0000	.0000	.0000
2	3.2500	15.0000	-.1000	.0000
3	13.2500	14.0000	-.2105	.0000
4	22.7500	12.0000	-.4444	.0000
5	25.0000	11.0000	.0000	.0000
6	27.2500	11.0000	-.2791	.0000
7	38.0000	8.0000	.0000	.0000
8	40.0000	8.0000	-.4444	.0000
9	42.2500	7.0000	-.4848	.0000
10	50.5000	3.0000	-.4286	.0000
11	57.5000	.0000	.0000	.0000
12	64.0000	.0000	.0000	.0000
13	70.2500	.0000	.1538	.0000
14	76.7500	1.0000	.3077	.0000
15	83.2500	3.0000	.3478	.0000
16	89.0000	5.0000	.3478	.0000
17	94.7500	7.0000	.3478	.0000
18	100.5000	9.0000	.1481	.0000
19	107.2500	10.0000	.3636	.0000
20	112.7500	12.0000	.1667	.0000
21	118.7500	13.0000	.1613	.0000
22	124.2500	14.0000	.1000	.0000
23	130.2500	14.0000	.0000	.0000
24	136.2500	14.0000	.0000	.0000
25	142.7500	14.0000	.0000	.0000
26	149.2500	14.0000	-.2759	.0000
27	156.5000	12.0000	.0000	.0000
28	162.7500	12.0000	.0000	.0000
29	170.0000	12.0000	.0000	.0000
30	177.2500	12.0000	-.1250	.0000
31	185.2500	11.0000	.0000	.0000
32	193.2500	11.0000	.1290	.0000
33	201.0000	12.0000	.0000	.0000
34	208.7500	12.0000	.1333	.0000
35	216.2500	13.0000	.1290	.0000
36	224.0000	14.0000	.1143	.0000
37	232.7500	15.0000	.0000	.0000
38	239.2500	15.0000	.0000	.0000
39	249.7500	15.0000	.0000	.0000
40	255.0000	15.0000	.0000	.0000

DIVIDED DIFFERENCE TABLE

1	.0000	-36.5000	-.4615	.0000
2	3.2500	-38.0000	-.4000	.0000
3	13.2500	-42.0000	-.4211	.0000
4	22.7500	-46.0000	-.4444	.0000
5	25.0000	-47.0000	-.4444	.0000
6	27.2500	-48.0000	12.6512	.0000
7	38.0000	88.0000	-.5000	.0000
8	40.0000	87.0000	-.4444	.0000
9	42.2500	86.0000	-.4848	.0000
10	50.5000	82.0000	-.5714	.0000
11	57.5000	78.0000	-.6154	.0000

12	64.0000	74.0000	-.6400	.0000
13	70.2500	70.0000	-.6154	.0000
14	76.7500	66.0000	-.6154	.0000
15	83.2500	62.0000	-.6957	.0000
16	89.0000	58.0000	-.6957	.0000
17	94.7500	54.0000	-.6957	.0000
18	100.5000	50.0000	-.5926	.0000
19	107.2500	46.0000	-.7273	.0000
20	112.7500	42.0000	-.6667	.0000
21	118.7500	38.0000	-.7273	.0000
22	124.2500	34.0000	-.6667	.0000
23	130.2500	30.0000	-.6667	.0000
24	136.2500	26.0000	-.6154	.0000
25	142.7500	22.0000	-.6154	.0000
26	149.2500	18.0000	-.5517	.0000
27	156.5000	14.0000	-.6400	.0000
28	162.7500	10.0000	-.5517	.0000
29	170.0000	6.0000	-.5517	.0000
30	177.2500	2.0000	-.5000	.0000
31	185.2500	-2.0000	-.5600	.0000
32	193.2500	-6.0000	-.5161	.0000
33	201.0000	-10.0000	-.5161	.0000
34	208.7500	-14.0000	-.5333	.0000
35	216.2500	-18.0000	-.5161	.0000
36	224.0000	-22.0000	-.4571	.0000
37	232.7500	-26.0000	-.6154	.0000
38	239.2500	-30.0000	-.5019	.0000
39	249.7500	-34.0000	-.7810	.0000
40	255.0000	-36.0000	.0000	.0000

OUTPUT DATA

TEMP	ADDRESS	LOC	RHOb
-36.5000	0	15	15.0000
-36.9615	1	15	15.0000
-37.4231	2	15	15.0000
-37.8846	3	15	15.0000
-38.3000	4	15	14.9250
-38.7000	5	15	14.8250
-39.1000	6	15	14.7250
-39.5000	7	15	14.6250
-39.9000	8	15	14.5250
-40.3000	9	14	14.4250
-40.7000	10	14	14.3250
-41.1000	11	14	14.2250
-41.5000	12	14	14.1250
-41.9000	13	14	14.0250
-42.3158	14	14	13.9421
-42.7368	15	14	13.8316
-43.1579	16	13	13.4211
-43.5789	17	13	13.2105
-44.0000	18	13	13.0000
-44.4211	19	13	12.7895
-44.8421	20	13	12.5789
-45.2632	21	13	12.3684
-45.6842	22	13	12.1579
-46.1111	23	12	11.8889
-46.5556	24	12	11.4444
-47.0000	25	11	11.0000
-47.4444	26	11	11.0000
-47.8889	27	11	11.0000
-38.5116	28	11	10.7907
-25.8605	29	11	10.5116
-15.2093	30	10	10.2326
-.558140	31	10	9.95349
12.0930	32	10	9.67442
24.7442	33	9	9.39535
37.3953	34	9	9.11628
50.0465	35	9	8.83721
62.6977	36	9	8.55814
75.3488	37	8	8.27907
88.0000	38	8	8.00000
87.5000	39	8	8.00000
87.0000	40	8	8.00000
86.5556	41	8	7.55556
86.1111	42	7	7.11111

OUTPUT DATA

TEMP	ADDRESS	INCH	RAICH
65.6364	43	7	6.63636
65.1515	44	6	6.15152
64.6667	45	6	6.66667
64.1818	46	5	5.18182
63.6970	47	5	4.69697
63.2121	48	4	4.21212
62.7273	49	4	3.72727
62.2424	50	3	3.24242
61.7143	51	3	2.78571
61.1429	52	2	2.35714
60.5714	53	2	1.92857
60.0000	54	2	1.50000
79.4286	55	1	1.07143
78.8571	56	1	.642857
78.2857	57	0	.214286
77.6923	58	0	0
77.0769	59	0	0
76.4615	60	0	0
75.8462	61	0	0
75.2308	62	0	0
74.6154	63	0	0
74.0000	64	0	0
73.3600	65	0	0
72.7200	66	0	0
72.0800	67	0	0
71.4400	68	0	0
70.8000	69	0	0
70.1600	70	0	0
69.5385	71	0	.115385
68.9231	72	0	.269231
68.3077	73	0	.423077
67.6923	74	1	.576923
67.0769	75	1	.730769
66.4615	76	1	.884615
65.8462	77	1	1.07692
65.2308	78	1	1.38462
64.6154	79	2	1.69231
64.0000	80	2	2.00000
63.3846	81	2	2.30769
62.7692	82	3	2.61538
62.1538	83	3	2.92308
61.4783	84	3	3.26087
60.7826	85	4	3.60870

OUTPUT DATA

TEMP	ADDRESS	LOW	RECK
60.0870	86	4	3.95652
59.3913	87	4	4.30435
58.6957	88	5	4.65217
58.0000	89	5	5.00000
57.3043	90	5	5.34783
56.6087	91	6	5.69565
55.9130	92	6	6.04348
55.2174	93	6	6.39130
54.5217	94	7	6.73913
53.8261	95	7	7.08696
53.1304	96	7	7.43478
52.4348	97	8	7.78261
51.7391	98	8	8.13043
51.0435	99	8	8.47826
50.3478	100	9	8.82609
49.7037	101	9	9.07407
49.1111	102	9	9.22222
48.5185	103	9	9.37037
47.9259	104	10	9.51852
47.3333	105	10	9.66667
46.7407	106	10	9.81481
46.1481	107	10	9.96296
45.4545	108	10	10.2727
44.7273	109	11	10.6364
44.0000	110	11	11.0000
43.2727	111	11	11.3636
42.5455	112	12	11.7273
41.8333	113	12	12.0417
41.1667	114	12	12.2083
40.5000	115	12	12.3750
39.8333	116	13	12.5417
39.1667	117	13	12.7083
38.5000	118	13	12.8750
37.8182	119	13	13.0455
37.0909	120	13	13.2273
36.3636	121	13	13.4091
35.6364	122	14	13.5909
34.9091	123	14	13.7727
34.1818	124	14	13.9545
33.5000	125	14	14.0000
32.8333	126	14	14.0000
32.1667	127	14	14.0000
31.5000	128	14	14.0000

OUTPUT DATA

TEMP	ADDRESS	NCA	ROCK
30.8333	129	14	14.0000
30.1667	130	14	14.0000
29.5000	131	14	14.0000
28.8333	132	14	14.0000
28.1667	133	14	14.0000
27.5000	134	14	14.0000
26.8333	135	14	14.0000
26.1667	136	14	14.0000
25.5385	137	14	14.0000
24.9231	138	14	14.0000
24.3077	139	14	14.0000
23.6923	140	14	14.0000
23.0769	141	14	14.0000
22.4615	142	14	14.0000
21.8462	143	14	14.0000
21.2308	144	14	14.0000
20.6154	145	14	14.0000
20.0000	146	14	14.0000
19.3846	147	14	14.0000
18.7692	148	14	14.0000
18.1538	149	14	14.0000
17.5862	150	14	13.7931
17.0345	151	14	13.5172
16.4828	152	13	13.2414
15.9310	153	13	12.9655
15.3793	154	13	12.6897
14.8276	155	12	12.4138
14.2759	156	12	12.1379
13.6800	157	12	12.0000
13.0400	158	12	12.0000
12.4000	159	12	12.0000
11.7600	160	12	12.0000
11.1200	161	12	12.0000
10.4800	162	12	12.0000
9.86207	163	12	12.0000
9.31034	164	12	12.0000
8.75862	165	12	12.0000
8.20690	166	12	12.0000
7.65517	167	12	12.0000
7.10345	168	12	12.0000
6.55172	169	12	12.0000
6.00000	170	12	12.0000
5.44828	171	12	12.0000

OUTPUT DATA

TEMP	ADDRESS	ROW	RHCK
4.89655	172	12	12.0000
4.34483	173	12	12.0000
3.79310	174	12	12.0000
3.24138	175	12	12.0000
2.68966	176	12	12.0000
2.13793	177	12	12.0000
1.62500	178	12	11.9062
1.12500	179	12	11.7812
.625000	180	12	11.6562
.125000	181	12	11.5312
-.375000	182	11	11.4062
-.875000	183	11	11.2812
-1.37500	184	11	11.1562
-1.87500	185	11	11.0312
-2.37500	186	11	11.0000
-2.87500	187	11	11.0000
-3.37500	188	11	11.0000
-3.87500	189	11	11.0000
-4.37500	190	11	11.0000
-4.87500	191	11	11.0000
-5.37500	192	11	11.0000
-5.87500	193	11	11.0000
-6.38710	194	11	11.0968
-6.90323	195	11	11.2258
-7.41935	196	11	11.3548
-7.93548	197	11	11.4839
-8.45161	198	12	11.6129
-8.96774	199	12	11.7419
-9.48387	200	12	11.8710
-10.0000	201	12	12.0000
-10.5161	202	12	12.0000
-11.0323	203	12	12.0000
-11.5484	204	12	12.0000
-12.0645	205	12	12.0000
-12.5806	206	12	12.0000
-13.0968	207	12	12.0000
-13.6129	208	12	12.0000
-14.1333	209	12	12.0333
-14.6667	210	12	12.1667
-15.2000	211	12	12.3000
-15.7333	212	12	12.4333
-16.2667	213	13	12.5667
-16.8000	214	13	12.7000

OUTPUT DATA

TEMP	ADDRESS	LOW	RDCV
-17.3333	215	13	12.8333
-17.8667	216	13	12.9667
-18.3871	217	13	13.0968
-18.9032	218	13	13.2258
-19.4194	219	13	13.3548
-19.9355	220	13	13.4839
-20.4516	221	14	13.6129
-20.9677	222	14	13.7419
-21.4839	223	14	13.8710
-22.0000	224	14	14.0000
-22.4571	225	14	14.1143
-22.9143	226	14	14.2286
-23.3714	227	14	14.3429
-23.8286	228	14	14.4571
-24.2857	229	14	14.5714
-24.7429	230	15	14.6857
-25.2000	231	15	14.8000
-25.6571	232	15	14.9143
-26.1538	233	15	15.0000
-26.7692	234	15	15.0000
-27.3846	235	15	15.0000
-28.0000	236	15	15.0000
-28.6154	237	15	15.0000
-29.2308	238	15	15.0000
-29.8462	239	15	15.0000
-30.2857	240	15	15.0000
-30.6667	241	15	15.0000
-31.0476	242	15	15.0000
-31.4286	243	15	15.0000
-31.8095	244	15	15.0000
-32.1905	245	15	15.0000
-32.5714	246	15	15.0000
-32.9524	247	15	15.0000
-33.3333	248	15	15.0000
-33.7143	249	15	15.0000
-34.0952	250	15	15.0000
-34.4762	251	15	15.0000
-34.8571	252	15	15.0000
-35.2381	253	15	15.0000
-35.6190	254	15	15.0000
-36.0000	255	15	15.0000

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FEB 77 A B MROCH, G R HYKES DAAB07-73-C-0137

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2 OF 2
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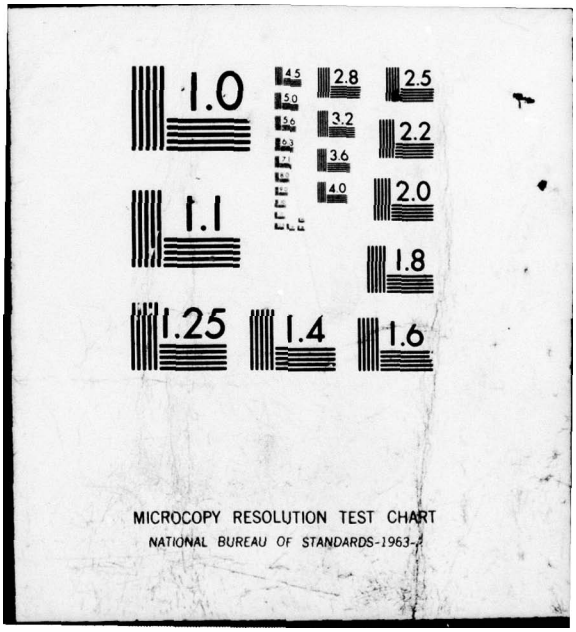
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5.0
5.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

```
**** PLOT DEBUG ****
   1 CURVES WERE SPECIFIED
 256 POINTS PER CURVE WERE SPECIFIED
MINIMUM X VALUE SPECIFIED =     0.0000000
MAXIMUM X VALUE SPECIFIED =     2.5500000+02
MINIMUM Y VALUE SPECIFIED =     0.0000000
MAXIMUM Y VALUE SPECIFIED =     1.5000000+01

INITIAL AND FINAL VALUES
X(1) =     0.0000000          X( 256) =     2.5500000+02
Y(1,  1) =     1.5000000+01     Y( 256,  1) =     1.5000000+01

****
**** PLOT DEBUG ****
   1 CURVES WERE SPECIFIED
  40 POINTS PER CURVE WERE SPECIFIED
MINIMUM X VALUE SPECIFIED =     0.0000000
MAXIMUM X VALUE SPECIFIED =     2.5500000+02
MINIMUM Y VALUE SPECIFIED =     0.0000000
MAXIMUM Y VALUE SPECIFIED =     1.5000000+01

INITIAL AND FINAL VALUES
X(1) =     0.0000000          X(  40) =     2.5500000+02
Y(1,  1) =     1.5000000+01     Y(  40,  1) =     1.5000000+01

****
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91/92

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TIME:     TOTAL: 00:01:45.261       CBSUPS:  029675055

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